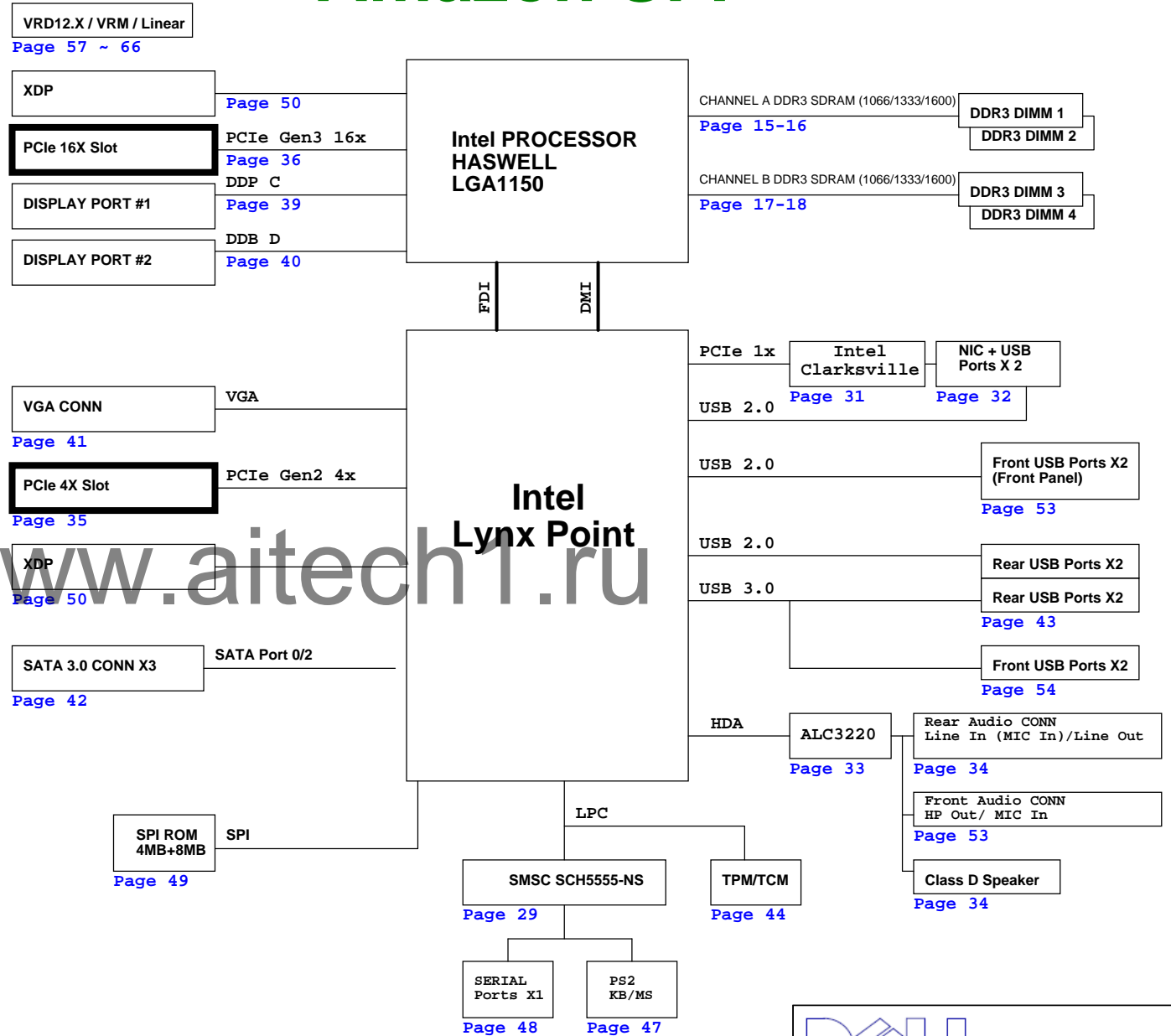


# Amazon SFF

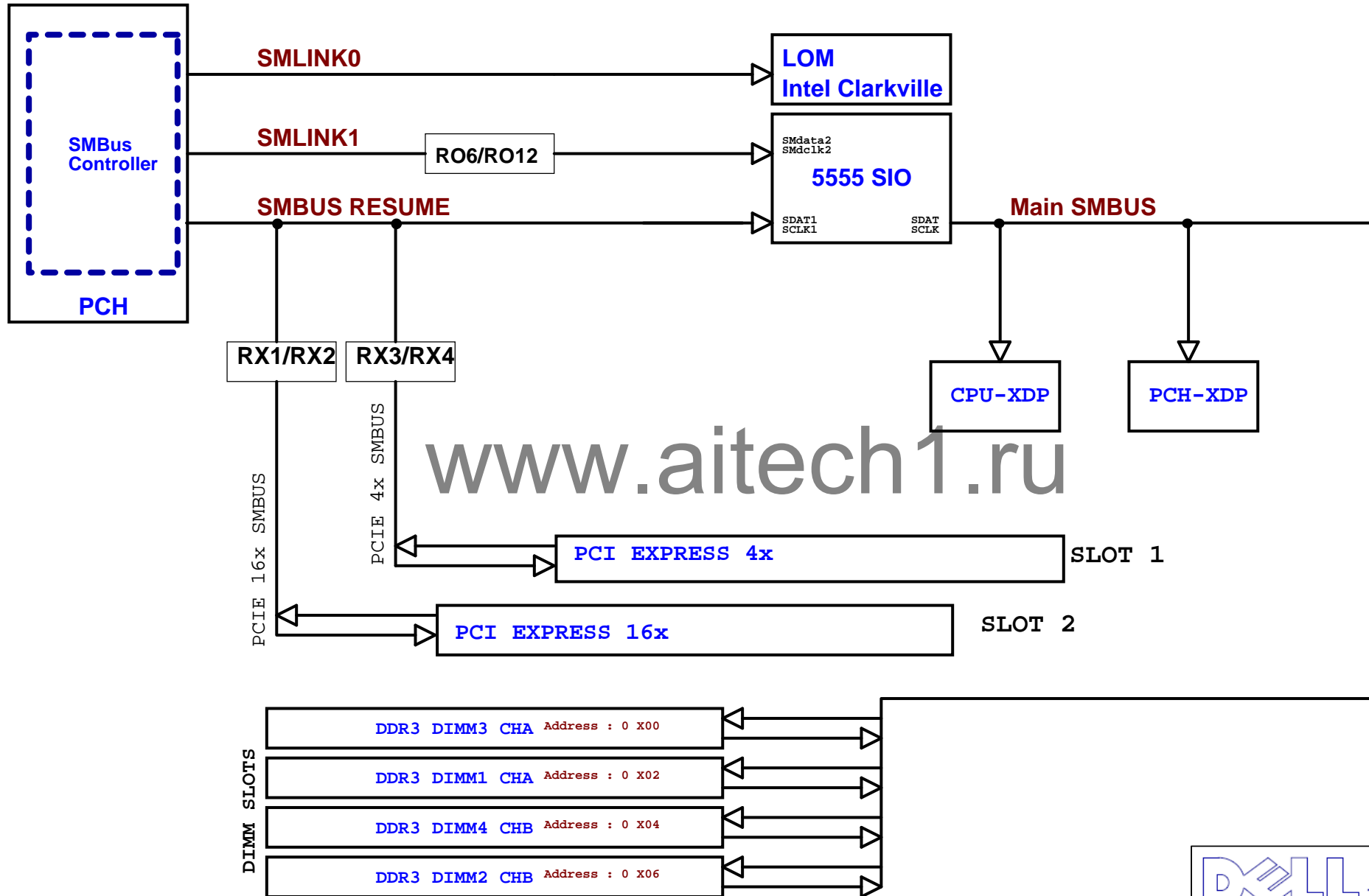
1. Index / Block diagram
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- 31-32. LAN: Intel Clarkville
- 33-34. AUDIO ALC3220
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37. TBD
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39. Display Port 1
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46. Thermal Sensor Conn
47. PS2 Conn
48. COM1
49. SPI
50. XDP
51. Pilot Run/LPC Debug/APS
52. EMI
53. Front Panel
54. Front USB3.0
55. TBD
56. TBD
57. Power Conn
58. Power Sequence
59. Power--> Linear 1
60. Power--> Linear 2
61. Power--> Linear 3
62. Power--> Vcore PWM
63. Power--> Vcore Driver
64. Power--> DDR3
65. Power--> 5VSB / +3VDUAL
66. Power--> -12V

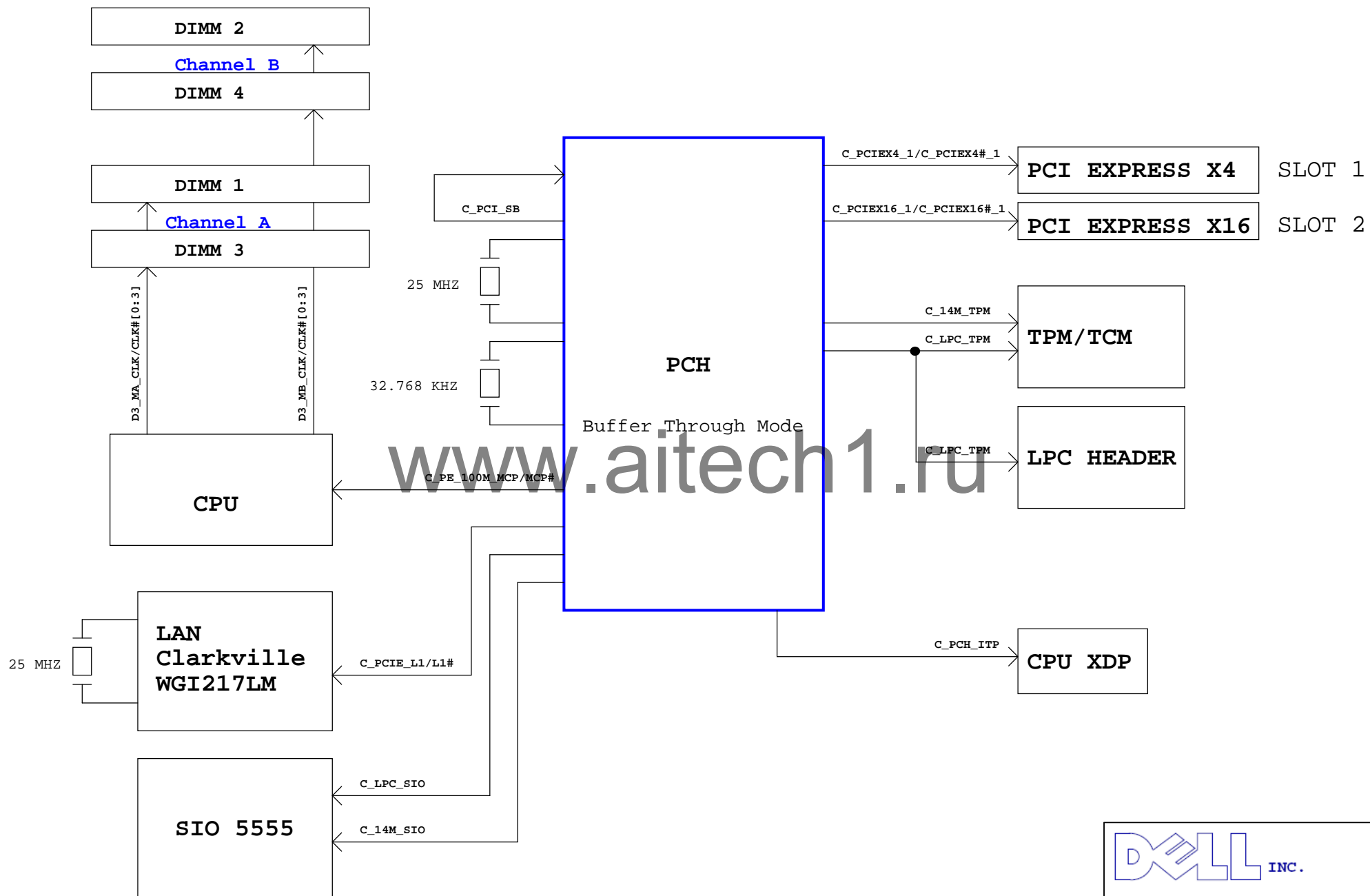


DESIGN	CHECK	APPROVE
Steven		

Title		
Index / Block diagram		
DWG NO	Rev	
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# SMBUS DIAGRAM





PSU

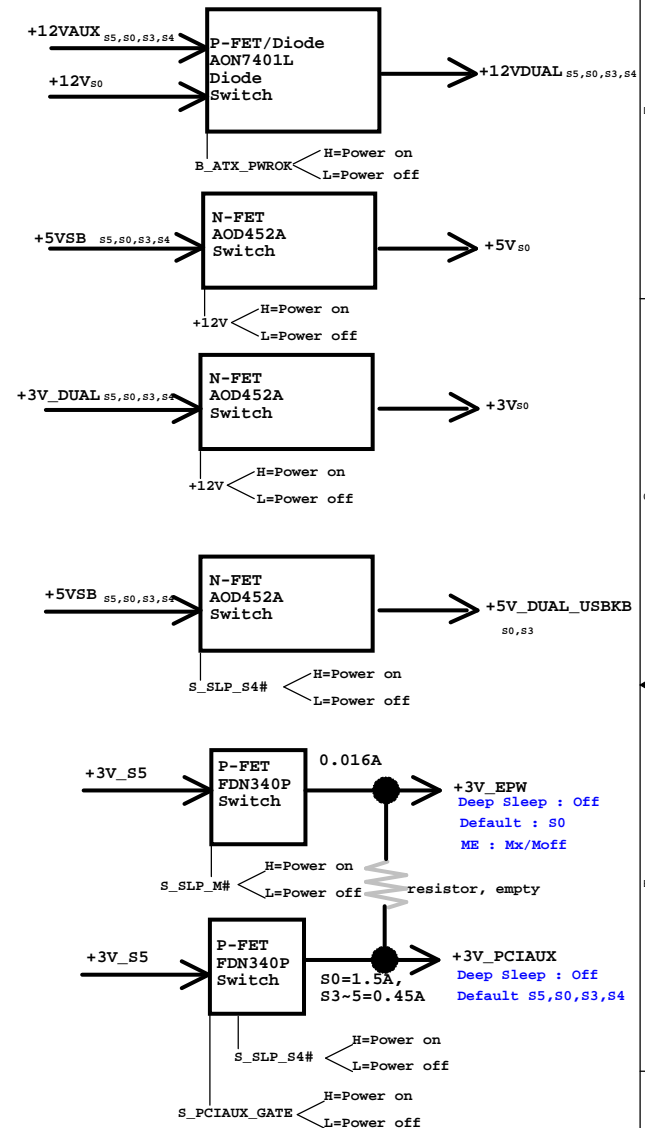
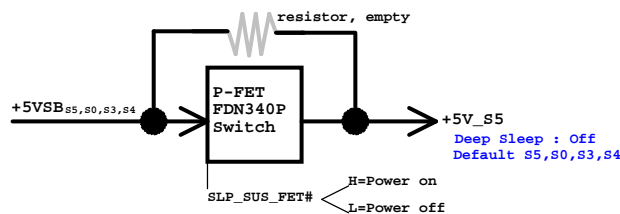
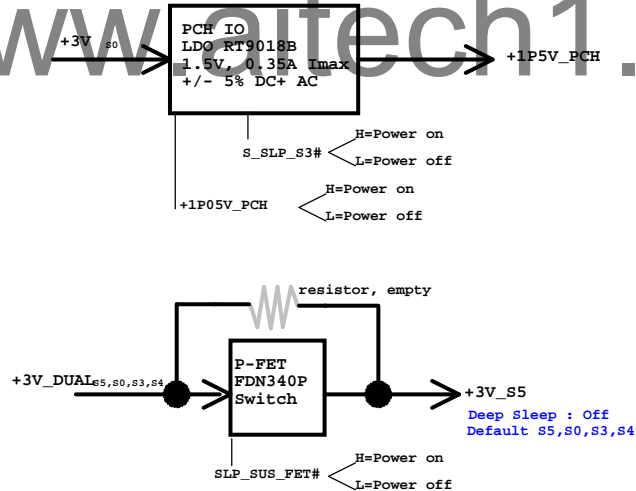
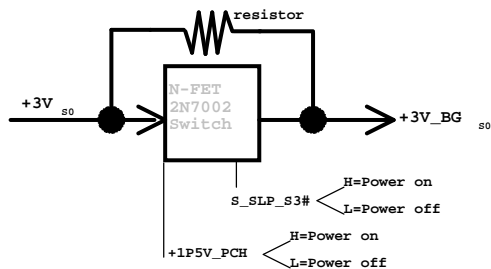
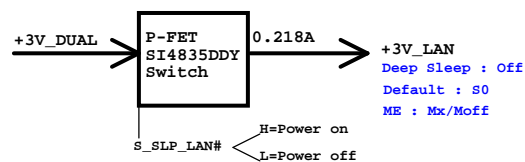
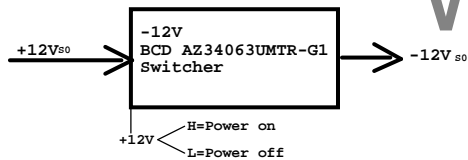
2X3

12V  $+12V_{AUX}$  <sup>S5,S0,S3,S4</sup>  
TBD A

12V  $+12V_{S0}$   
TBD A

2X2

12V  $+12V_{CPU,S0}$   
TBD A



### Power Delivery Map

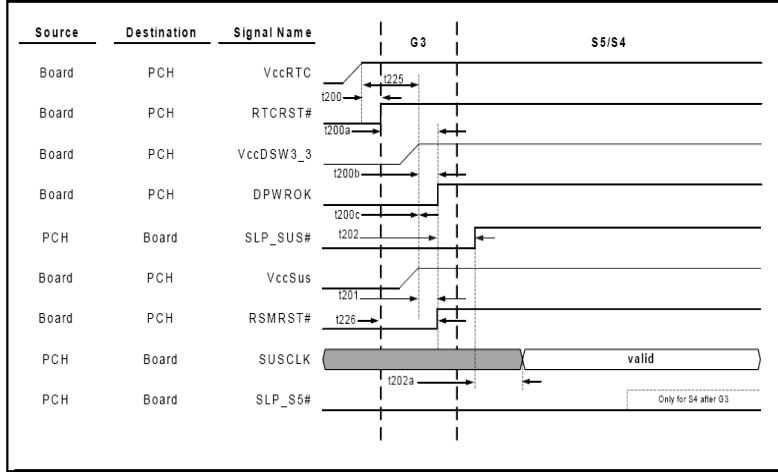
## Amazon SFF

Rev **A00**

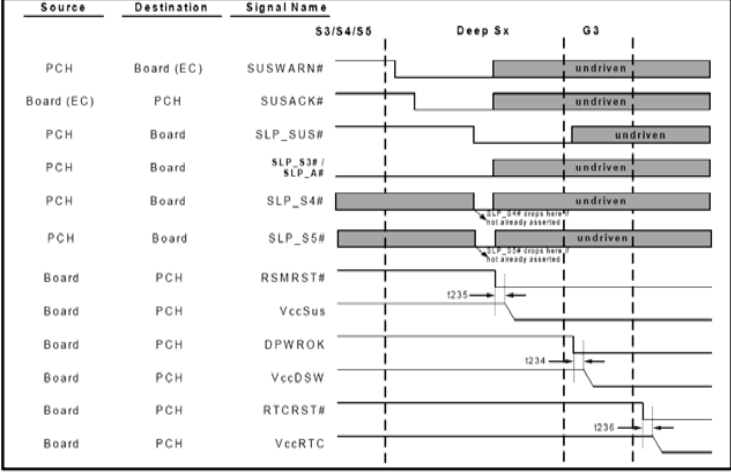
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POWER ON Timing Diagram

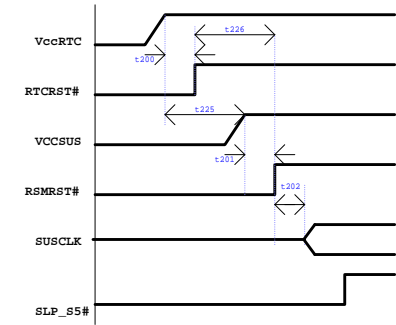
G3 --> S4/S5 (with Deep Sleep support)



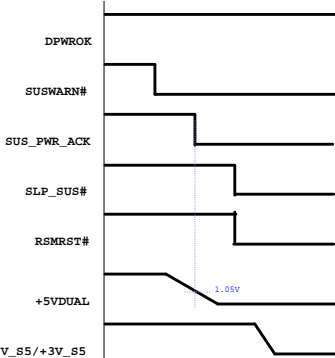
Sx --> Deep S4/S5 -->G3



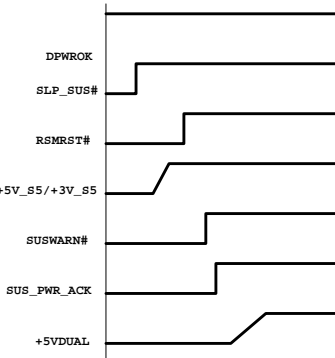
G3 to S4/S5 Timing Diagram



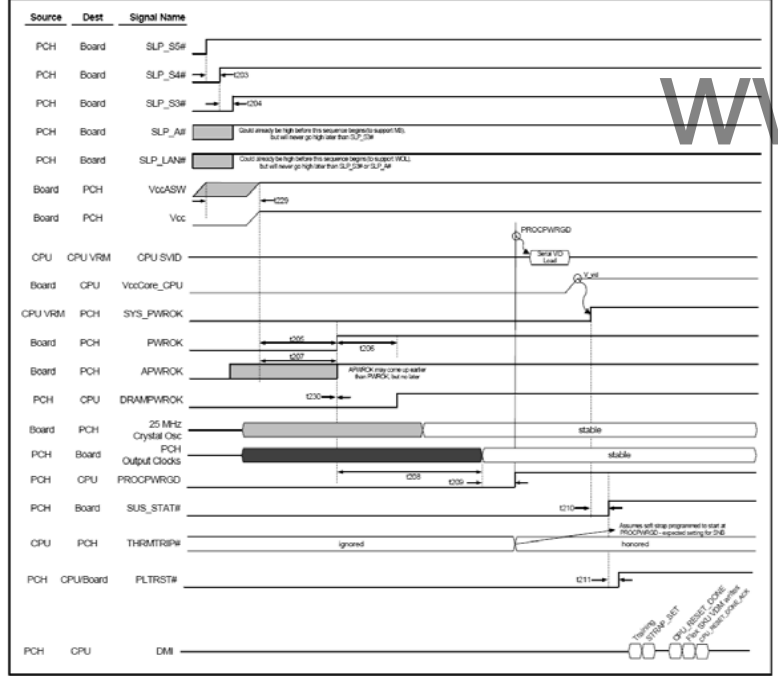
Deep Sleep Entry



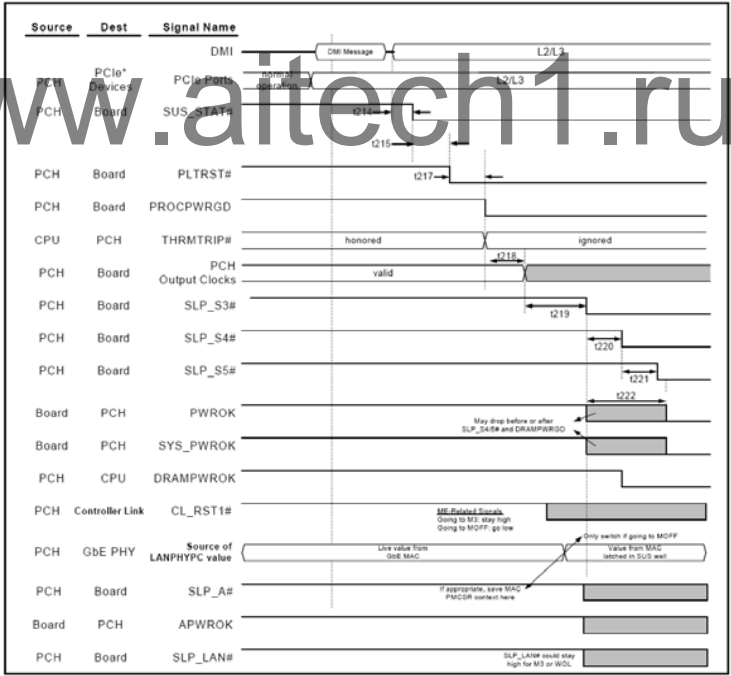
Deep Sleep Exit



S5 --> S0



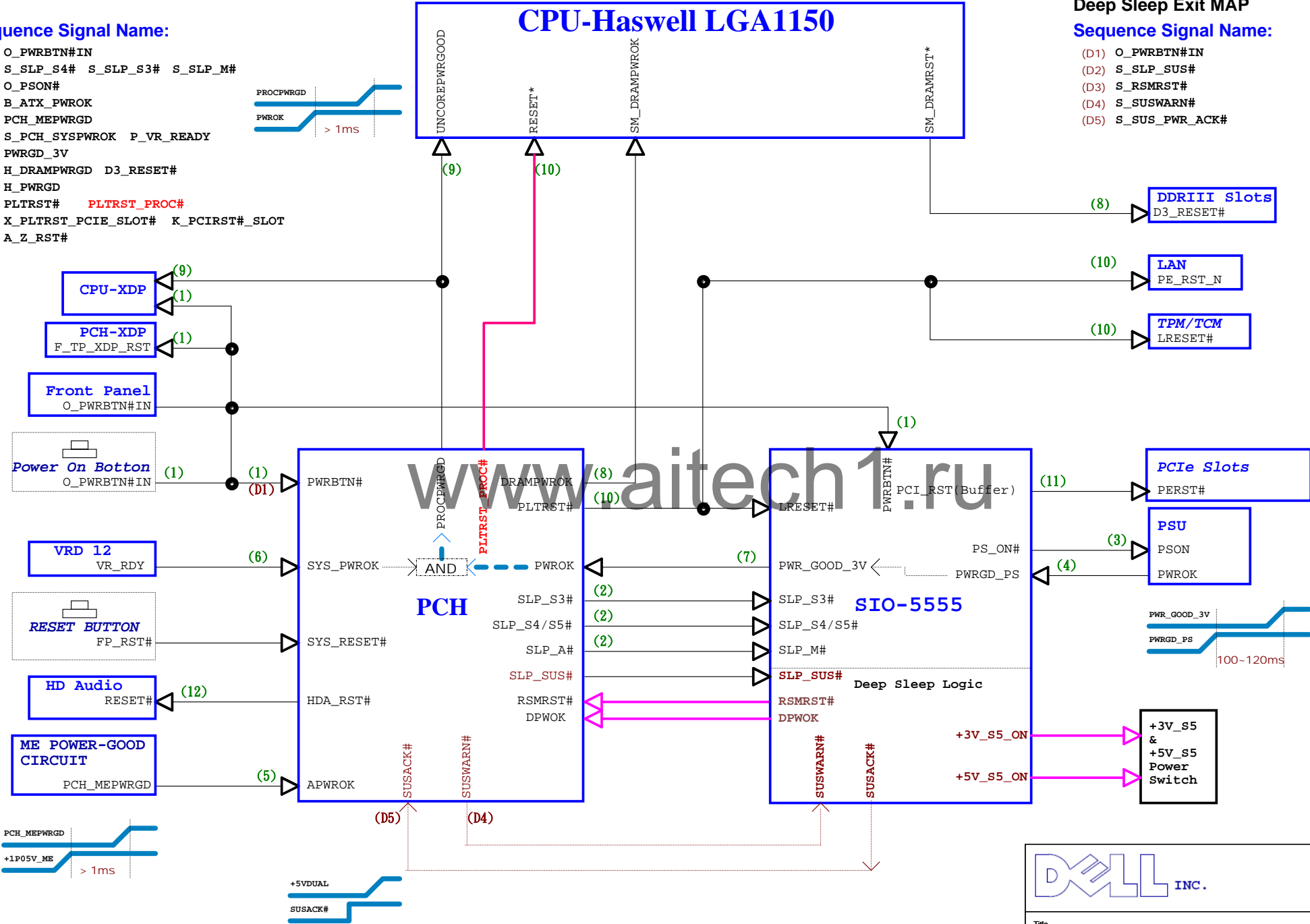
S0 --> S5



RESET / Power Good MAP

Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWROGD
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWROGD D3\_RESET#
- (9) H\_PWROGD
- (10) PLTRST# PLTRST\_PROG#
- (11) X\_PLTRST\_PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O\_PWRBTN#IN
- (D2) S\_SLP\_SUS#
- (D3) S\_RSMRST#
- (D4) S\_SUSWARN#
- (D5) S\_SUS\_PWR\_ACK#

## STRAPPING Table

## PCH side

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	<b>Default Mode:</b> Internal weak Pull-down.  <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPI055	I/O	<b>Default Mode:</b> Internal pull-up.  <b>Top Block Swap Mode:</b> Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPI019, GPI051	I/O	<b>Default (SPI)</b> Left both SATA1GP/GPI019 and GPI051 floating. No pull up required.  <b>Boot from PCI</b> Connect SATA1GP/GPI019 to ground with 1k Ohm pull-down resistor. Leave GPI051 Floating.  <b>Boot from LPC</b> Connect both SATA1GP/GPI019 and GPI051 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.  Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPI053	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ES1 strap for server platform ONLY
HDA_SDO	I/O	<b>Default</b> Do not pull high.  <b>Disable ME in Manufacturing Mode</b> Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down. Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPI037	I/O	<b>Enable TLS:</b> Pull up with 1k Ohm to VccSus3.3. <b>Default (Disable TLS):</b> Leave NC. Internal pull down.	TLS confidentiality
GPI08	I/O	Internal weak pull up. Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPI062/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPI036	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA		Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

## CPU side

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	<b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"> <li>• <b>CFG[1:0]:</b> Reserved configuration lane. A test point may be placed on the board for this lane.</li> <li>• <b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal               <ul style="list-style-type: none"> <li>~ x1 = Normal operation</li> <li>~ x0 = Lane numbers reversed</li> </ul> </li> <li>• <b>CFG[3]:</b> PCI Express* Static x4 Lane Numbering Reversal               <ul style="list-style-type: none"> <li>~ x1 = Normal operation</li> <li>~ x0 = Lane numbers reversed</li> </ul> </li> <li>• <b>CFG[4]:</b> Reserved configuration lane. A test point may be placed on the board for this lane.</li> <li>• <b>CFG[6:5]: PCI Express* Bifurcation:</b><sup>1</sup> <ul style="list-style-type: none"> <li>~ x00 = 1 x8, 2 x4 PCI Express*</li> <li>~ x01 = reserved</li> <li>~ x10 = 2 x8 PCI Express*</li> <li>~ x11 = 1 x16 PCI Express*</li> </ul> </li> <li>• <b>CFG[19:7]:</b> Reserved configuration lanes. A test point may be placed on the board for these lands.</li> </ul>	I CMOS

## Strapping Options Flash

GNT1#	SATA1GP/GPI019	Routing
0	0	Flash Cycles Routed to LPC
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPB_CTRLCLK	Straps for digital ports B, C and D.  For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port.  For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2KW resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch.  For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2KW resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

## SIO SMSC5555

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable <span style="color: red;">DEFAULT</span>



Title		
GPIO/IRQ/IDSEL Table		
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Amazon SFF		
Date: Tuesday, March 12, 2013	Sheet 7 of	66

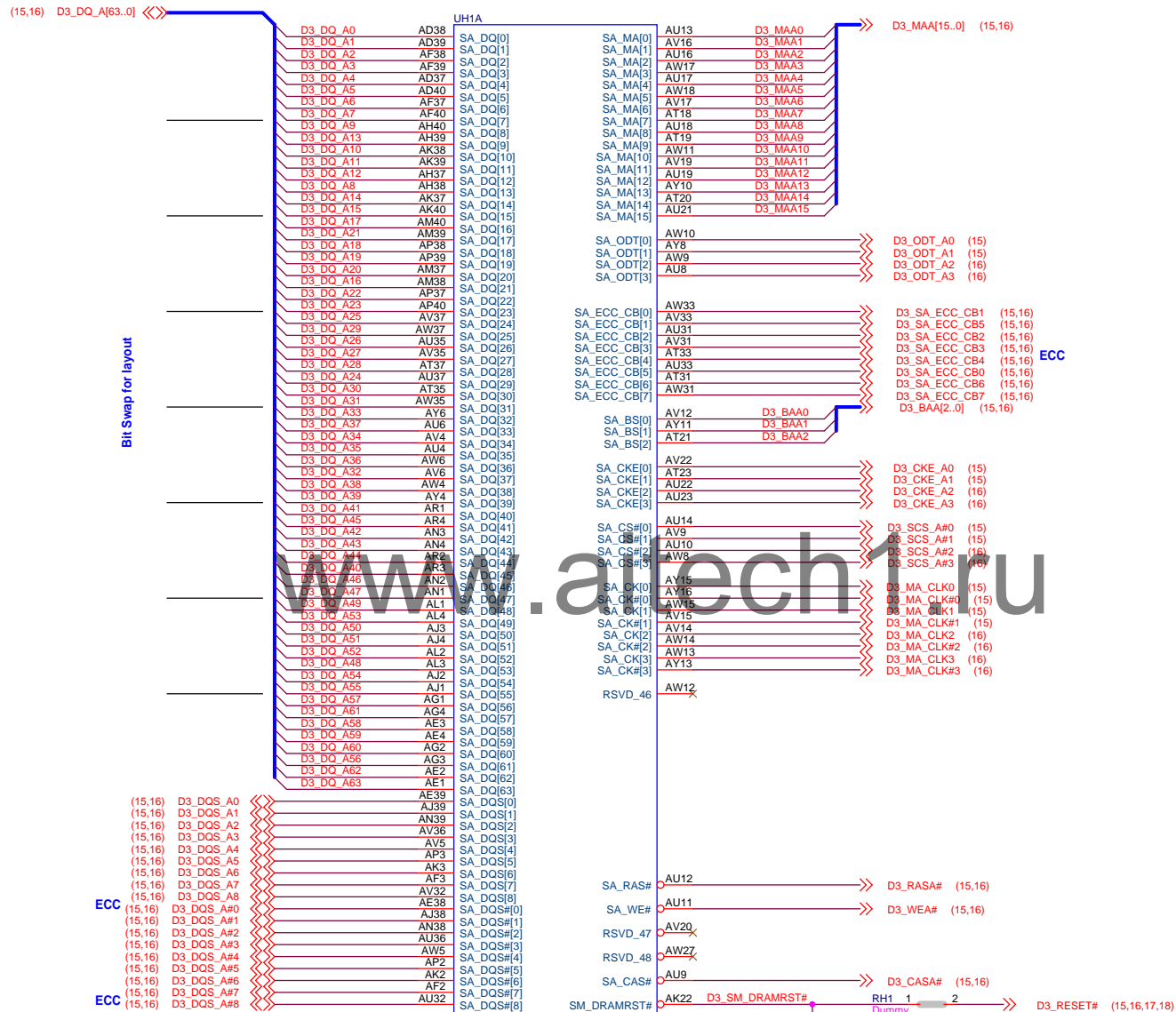


PCH GPIO Summary									
GPIO	Mult Function Pin	PIN OUT	Type	Power Well	Default	Signal Name	IN-PU/PD	EX-PU/PD	*Current Usage I/O/N/A/NotUsed/Strapping
GPIO0	BM518/GPI00	G38	VO	Core	GPIO	S_PECI_RE0R	--	10k pull-up to +V <sub>V</sub>	I
GPIO1	TACH1/GPI01	A731	VO	Core	GPIO	S_OPI_CHASIS_ID0	20K IN-PU (only on TACH1)	10k pull-up to +V <sub>V</sub> 10k pull-down to GND (dummy)	I
GPIO2	PIR0M/GPI02	A630	VOD	Core	GPIO	S_OPI02	--	0.2k pull-up to +V <sub>V</sub>	NU
GPIO3	PIR0F/GPI03	A629	VOD	Core	GPIO	V_DD0P_C_HPD	--	--	I
GPIO4	PIR0M/GPI04	A629	VOD	Core	GPIO	V_OPI_VSA_CBL_DET#	--	0.2k pull-up to +V <sub>V</sub>	I
GPIO5	PIR0H/GPI05	A727	VOD	Core	GPIO	S_OPI05	--	0.2k pull-up to +V <sub>V</sub>	NU
GPIO6	TACH2/GPI06	A628	VO	Core	GPIO	S_OPI06	20K IN-PU (only on TACH2)	10k pull-up to +V <sub>V</sub>	NU
GPIO7	TACH3/GPI07	A604	VO	Core	GPIO	S_OPI_SKU2	20K IN-PU (only on TACH3)	10k pull-up to +V <sub>V</sub> (dummy) 22k pull-down to GND	I
GPIO8	GPI08	AC40	Suspend	GPO	GPIO	S_J0C_BLM	20K IN-PU	--	NU (connected to XDP_PCH)
GPIO9	OC5M/GPI09	AC41	VO	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO10	OC6M/GPI10	AF40	VO	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO11	SMBALET/GPI011	AQ31	VO	Suspend	Native	X4_WA#E#	--	10k pull-up to +V <sub>V</sub> , S5	I
GPIO12	LMB_RST_PCH_CTRL/GPI012	A640	VOD	Suspend	Native	S_LMB_RST_HB0R	--	10k pull-up to +V <sub>V</sub> , LMB 10k pull-down to GND (dummy)	I
GPIO13	GPIO13	A623	VOD	Suspend	GPIO	S_OPI013	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO14	OC6M/GPI014	A640	VOD	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO15	GPIO15	A624	VOD	Suspend	GPO	S_OPI015	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO16	SATA0SR/GPI016	A629	VO	Core	GPIO	S_SATA0SR	--	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO17	TACH0M/GPI017	A628	VO	Core	GPIO	S_OPI017	20K IN-PU (only on TACH0M)	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	I
GPIO18	PCIECLKREQ/GPI018	F036	VOD	Core	Native	S_OPI018	--	10k pull-up to +V <sub>V</sub> (connected to XDP_PCH)	NU
GPIO19	SATA0SR/GPI019	J460	VOD	Core	GPIO	S_SATA0SR	20K IN-PU	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO20	PCIECLKREQ/GPI020	F037	VOD	Core	Native	S_OPI020	--	10k pull-up to +V <sub>V</sub> (connected to XDP_PCH)	NU
GPIO21	SATA0SR/GPI021	A627	VO	Core	GPIO	S_SATA0SR	20K IN-PU (only on TACH0M)	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	I
GPIO22	SATA0SR/GPI022	L28	VOD	Core	GPIO	S_SATA0SR	--	10k pull-up to +V <sub>V</sub> 4.7k pull-down to GND (dummy)	I
GPIO23	GPIO23	A626	VOD	Core	Native	S_OPI023	20K IN-PU	--	NU
GPIO24	GPIO24	A624	VOD	Suspend	GPO	S_OPI024	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO25	PCIECLKREQ/GPI025	A629	VOD	Suspend	Native	S_OPI025	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO26	PCIECLKREQ/GPI026	A629	VOD	Suspend	Native	S_OPI026	--	10k pull-up to +V <sub>V</sub> , S5	I
GPIO27	GPIO27	A624	VOD	Deep Sleep	GPIO	S_LMB_RST_HB0R	20K IN-PU	4.7k pull-up to +V <sub>V</sub> , S5	I
GPIO28	GPIO28	---	VOD	Suspend	GPO	S_OPI028	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO29	SUP_WAKEUP/GPI029	AC29	VO	Suspend	GPIO	S_OPI029	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO30	SUSWRNMSUSPWRNACK/GPI030	AQ41	VOD	Suspend	Native	S_SUSWRNMSUSPWRNACK	--	--	Native
GPIO31	GPIO31	A629	VOD	Deep Sleep	GPIO	S_OPI031	20K IN-PU	0.2k pull-up to +V <sub>V</sub> , S5	I
GPIO32	GPIO32	---	VOD	Core	GPO	S_OPI032	--	10k pull-up to +V <sub>V</sub> (dummy) 22k pull-down to GND	I
GPIO33	GPIO33	A624	VOD	Core	GPO	S_OPI033	PD	--	NU
GPIO34	GPIO34	---	VOD	Core	GPIO	S_OPI034	--	10k pull-up to +V <sub>V</sub>	NU
GPIO35	GPIO35	A640	VOD	Core	GPIO	S_OPI035	--	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND	I
GPIO36	SATA0SR/GPI036	A629	VOD	Core	GPIO	S_OPI036	20K IN-PU	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO37	SATA0SR/GPI037	A641	VOD	Core	GPIO	S_OPI037	20K IN-PU	10k pull-up to +V <sub>V</sub> 10k pull-down to GND (dummy)	Strapping
GPIO38	SATA0SR/GPI038	A641	VOD	Core	GPIO	S_OPI038	--	10k pull-up to +V <sub>V</sub> 10k pull-down to GND (dummy)	I
GPIO39	SATA0SR/GPI039	F031	VOD	Core	GPIO	A_LTP_PRES#	--	10k pull-up to +V <sub>V</sub>	I
GPIO40	OC6M/GPI040	AF37	VOD	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO41	OC5M/GPI041	A628	VOD	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO42	OC6M/GPI042	A640	VOD	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO43	OC6M/GPI043	AF38	VOD	Suspend	Native	U_USB_OC_R#	--	--	Native
GPIO44	PCIECLKREQ/GPI044	A628	VOD	Suspend	Native	S_OPI044	20K IN-PU	10k pull-up to +V <sub>V</sub> , S5	I
GPIO45	PCIECLKREQ/GPI045	A623	VOD	Suspend	Native	S_OPI045	--	10k pull-up to +V <sub>V</sub> , S5	NU

GPIO46	PCIECLKREQ/GPI046	A640	VOD	Suspend	Native	S_OPI046	20K IN-PU	10k pull-up to +V <sub>V</sub> , S5 (dummy) 10k pull-down to GND	I
GPIO47	GPIO47	A623	VOD	Core	GPIO	S_OPI047	--	--	I
GPIO48	SATA0SR/GPI048	A629	VOD	Core	GPIO	S_OPI048	--	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND	Strapping
GPIO49	GPIO49	A628	VOD	Core	GPIO	S_OPI049	--	10k pull-up to +V <sub>V</sub>	NU
GPIO50	GPIO50	A623	VOD	Core	GPIO	S_OPI050	20K IN-PU	10k pull-up to +V <sub>V</sub> (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO51	GPIO51	A623	VOD	Core	GPIO	S_OPI051	--	10k pull-up to +V <sub>V</sub>	NU
GPIO52	GPIO52	A628	VOD	Core	GPIO	S_OPI052	--	10k pull-up to +V <sub>V</sub>	NU
GPIO53	GPIO53	A623	VOD	Core	GPIO	S_OPI053	20K IN-PU	10k pull-up to GND (dummy)	Strapping
GPIO54	GPIO54	A623	VOD	Core	GPIO	S_OPI054	--	10k pull-up to +V <sub>V</sub>	NU
GPIO55	GPIO55	A628	VOD	Core	GPIO	S_OPI055	20K IN-PU	4.7k pull-up to GND (dummy)	Strapping
GPIO56	GPIO56	AC28	VOD	Suspend	GPIO	S_OPI056	--	10k pull-up to +V <sub>V</sub> , S5	NU
GPIO57	GPIO57	A628	VOD	Suspend	Native	S_OPI057	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO58	GPIO58	A628	VOD	Suspend	Native	S_OPI058	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO59	GPIO59	A628	VOD	Suspend	Native	S_OPI059	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO60	GPIO60	A628	VOD	Suspend	Native	S_OPI060	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO61	GPIO61	A628	VOD	Suspend	Native	S_OPI061	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO62	GPIO62	A628	VOD	Suspend	Native	S_OPI062	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO63	GPIO63	A628	VOD	Suspend	Native	S_OPI063	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO64	GPIO64	A628	VOD	Suspend	Native	S_OPI064	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO65	GPIO65	A628	VOD	Suspend	Native	S_OPI065	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO66	GPIO66	A628	VOD	Suspend	Native	S_OPI066	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO67	GPIO67	A628	VOD	Suspend	Native	S_OPI067	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO68	GPIO68	A628	VOD	Suspend	Native	S_OPI068	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO69	GPIO69	A628	VOD	Suspend	Native	S_OPI069	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO70	GPIO70	A628	VOD	Suspend	Native	S_OPI070	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO71	GPIO71	A628	VOD	Suspend	Native	S_OPI071	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO72	GPIO72	A628	VOD	Suspend	Native	S_OPI072	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO73	GPIO73	A628	VOD	Suspend	Native	S_OPI073	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO74	GPIO74	A628	VOD	Suspend	Native	S_OPI074	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO75	GPIO75	A628	VOD	Suspend	Native	S_OPI075	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO76	GPIO76	A628	VOD	Suspend	Native	S_OPI076	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO77	GPIO77	A628	VOD	Suspend	Native	S_OPI077	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO78	GPIO78	A628	VOD	Suspend	Native	S_OPI078	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO79	GPIO79	A628	VOD	Suspend	Native	S_OPI079	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO80	GPIO80	A628	VOD	Suspend	Native	S_OPI080	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO81	GPIO81	A628	VOD	Suspend	Native	S_OPI081	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO82	GPIO82	A628	VOD	Suspend	Native	S_OPI082	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO83	GPIO83	A628	VOD	Suspend	Native	S_OPI083	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO84	GPIO84	A628	VOD	Suspend	Native	S_OPI084	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO85	GPIO85	A628	VOD	Suspend	Native	S_OPI085	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO86	GPIO86	A628	VOD	Suspend	Native	S_OPI086	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO87	GPIO87	A628	VOD	Suspend	Native	S_OPI087	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO88	GPIO88	A628	VOD	Suspend	Native	S_OPI088	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO89	GPIO89	A628	VOD	Suspend	Native	S_OPI089	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO90	GPIO90	A628	VOD	Suspend	Native	S_OPI090	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO91	GPIO91	A628	VOD	Suspend	Native	S_OPI091	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO92	GPIO92	A628	VOD	Suspend	Native	S_OPI092	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO93	GPIO93	A628	VOD	Suspend	Native	S_OPI093	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO94	GPIO94	A628	VOD	Suspend	Native	S_OPI094	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO95	GPIO95	A628	VOD	Suspend	Native	S_OPI095	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO96	GPIO96	A628	VOD	Suspend	Native	S_OPI096	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO97	GPIO97	A628	VOD	Suspend	Native	S_OPI097	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO98	GPIO98	A628	VOD	Suspend	Native	S_OPI098	--	2.2k pull-up to +V <sub>V</sub> , S5	Native
GPIO99	GPIO99	A628	VOD	Suspend	Native	S_OPI099	--	2.2k pull-up to +V <sub>V</sub> , S5	Native

SIO 5555 GPIO Summary									
GPIO	PIN NAME	PIN OUT	Power well	Buffer Type	Signal Name	EX-PU/PD	*Current Usage I/O/N/A/NotUsed/Strapping	Programming Function	
GPIO0	GPIO0	4	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	Native	NA	
GPIO1	GPIO1	5	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	Native	NA	
GPIO2	GPIO2	7	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	Native	NA	
GPIO3	GPIO3	6	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	Native	NA	
GPIO4	SUSWRNMS / GPIO4	70	V <sub>0</sub> , V <sub>5</sub>	IO4	S_SUSWRNMS	NA	Native	NA	
GPIO5	HLCPURST0 / PECIAL_REQUEST#	22	V <sub>0</sub> , V <sub>5</sub>	IO8	O_PECIAL_REQUEST#	10k pull-up to +V <sub>V</sub>	Native	NA	
GPIO6	YELLOW# / GPIO6	25	V <sub>0</sub> , V <sub>5</sub>	IO8	O_YELLOW#	40k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO7	GREEN# / GPIO7	26	V <sub>0</sub> , V <sub>5</sub>	IO8	O_GREEN#	40k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO8	BLUEV# / GPIO8	27	V <sub>0</sub> , V <sub>5</sub>	IO8	S_BLUEV#	2.2k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO9	SMCLK# / GPIO9	28	V <sub>0</sub> , V <sub>5</sub>	IO8	S_SMCLK#	2.2k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO10	SPWRCK# / GPIO10	30	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SPWRCK#	10k pull-down to GND	Native	NA	
GPIO11	DMN_SHFT# / GPIO11	35	V <sub>0</sub> , V <sub>5</sub>	IO4	DMN_SHFT#	0.2k pull-up to +V <sub>V</sub> , S5 22k pull-down to GND (dummy)	I	1. default 0. Trim down adjustment	
GPIO12	PARSTRM# / GPIO12	36	V <sub>0</sub> , V <sub>5</sub>	IO4	O_PARSTRM#	1k pull-up to +V <sub>V</sub> , S5 (dummy)	Native	NA	
GPIO13	PROCHOT_IN# / PROCHOT_OUT# / GPIO13	39	V <sub>0</sub> , V <sub>5</sub>	LVMO24	H_PROCHOT	10k pull-up to H_CPU_VCCIO_RIC	Native	NA	
GPIO14	TACH1 / GPIO14	39	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SEN_CUFAN	1k pull-up to +V <sub>V</sub>	Native	NA	
GPIO15	TACH2 / GPIO15	40	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SEN_CUFAN	1k pull-up to +V <sub>V</sub>	Native	NA	
GPIO16	TACH3 / GPIO16	41	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	NU	NA	
GPIO17	PMM# / GPIO17	40	V <sub>0</sub> , V <sub>5</sub>	IO4	O_CUFAN_PMM	4.7k pull-up to +V <sub>V</sub>	Native	NA	
GPIO18	PMM# / GPIO18	40	V <sub>0</sub> , V <sub>5</sub>	IO4	O_CUFAN_PMM	4.7k pull-up to +V <sub>V</sub>	Native	NA	
GPIO19	PMM# / GPIO19	40	V <sub>0</sub> , V <sub>5</sub>	IO4	O_CUFAN_PMM	4.7k pull-up to +V <sub>V</sub>	Native	NA	
GPIO20	PMM# / GPIO20	40	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	NU	NA	
GPIO21	FP_CK_DET# / GPIO21	52	V <sub>0</sub> , V <sub>5</sub>	IO4	O_FP_CK_DET#	0.2k pull-up to +V <sub>V</sub> , S5	I	1. default 0. power switch cable plugged	
GPIO22	PCURST_V1# / GPIO22	63	V <sub>0</sub> , V <sub>5</sub>	IO4	X_PCURST_V1#_L0R#	Native	Native	NA	
GPIO23	PCURST_V2# / GPIO23	64	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	Native	NA	
GPIO24	PS_ON# / GPIO24	65	V <sub>0</sub> , V <sub>5</sub>	IO4	O_PS_ON#	4.7k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO25	PCURST_V3# / GPIO25	66	V <sub>0</sub> , V <sub>5</sub>	IO4	O_PCURST_V3#_DET#	0.2k pull-up to +V <sub>V</sub> , S5	I	1. default 0. PC speaker cable plugged	
GPIO26	SUSV_ON# / GPIO26	58	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SUS_V3#_ON	Native	Native	NA	
GPIO27	PMM# / GPIO27 / GPIO28	60	V <sub>0</sub> , V <sub>5</sub>	IO4	PMMREQ_2V#	NA	Native	NA	
GPIO28	SEMISTRM# / GPIO28	60	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SEMISTRM#	NA	NU	NA	
GPIO29	LATCHED_SEM_CUT# / GPIO29	60	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SEMISTRM#	NA	NU	NA	
GPIO30	SEMISTRM# / GPIO30	72	V <sub>0</sub> , V <sub>5</sub>	IO8	NC	NA	NU	NA	
GPIO31	GPIO31 / SEMI_CUT#	74	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	NU	NA	
GPIO32	GPIO32 / SEMI_CUT#	74	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	NU	NA	
GPIO33	GPIO33 / F10_PMEM	77	V <sub>0</sub> , V <sub>5</sub>	IO4	O_PMEM	10k pull-up to +V <sub>V</sub> , S5	Native	NA	
GPIO34	GPIO34	78	V <sub>0</sub> , V <sub>5</sub>	IO4	NC	NA	NU	NA	
GPIO35	SDCM# / GPIO35	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO36	SDCM# / GPIO36	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO37	SDCM# / GPIO37	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO38	SDCM# / GPIO38	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO39	SDCM# / GPIO39	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO40	SDCM# / GPIO40	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO41	SDCM# / GPIO41	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO42	SDCM# / GPIO42	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO43	SDCM# / GPIO43	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO44	SDCM# / GPIO44	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO45	SDCM# / GPIO45	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO46	SDCM# / GPIO46	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO47	SDCM# / GPIO47	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO48	SDCM# / GPIO48	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO49	SDCM# / GPIO49	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO50	SDCM# / GPIO50	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO51	SDCM# / GPIO51	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO52	SDCM# / GPIO52	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO53	SDCM# / GPIO53	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO54	SDCM# / GPIO54	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO55	SDCM# / GPIO55	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO56	SDCM# / GPIO56	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO57	SDCM# / GPIO57	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO58	SDCM# / GPIO58	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO59	SDCM# / GPIO59	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO60	SDCM# / GPIO60	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO61	SDCM# / GPIO61	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO62	SDCM# / GPIO62	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO63	SDCM# / GPIO63	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO64	SDCM# / GPIO64	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO65	SDCM# / GPIO65	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO66	SDCM# / GPIO66	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO67	SDCM# / GPIO67	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO68	SDCM# / GPIO68	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO69	SDCM# / GPIO69	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO70	SDCM# / GPIO70	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO71	SDCM# / GPIO71	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO72	SDCM# / GPIO72	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO73	SDCM# / GPIO73	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO74	SDCM# / GPIO74	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO75	SDCM# / GPIO75	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO76	SDCM# / GPIO76	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO77	SDCM# / GPIO77	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO78	SDCM# / GPIO78	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO79	SDCM# / GPIO79	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO80	SDCM# / GPIO80	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO81	SDCM# / GPIO81	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO82	SDCM# / GPIO82	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO83	SDCM# / GPIO83	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO84	SDCM# / GPIO84	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO85	SDCM# / GPIO85	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO86	SDCM# / GPIO86	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO87	SDCM# / GPIO87	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO88	SDCM# / GPIO88	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO89	SDCM# / GPIO89	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO90	SDCM# / GPIO90	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO91	SDCM# / GPIO91	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO92	SDCM# / GPIO92	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO93	SDCM# / GPIO93	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO94	SDCM# / GPIO94	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO95	SDCM# / GPIO95	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO96	SDCM# / GPIO96	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO97	SDCM# / GPIO97	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO98	SDCM# / GPIO98	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO99	SDCM# / GPIO99	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO100	SDCM# / GPIO100	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO101	SDCM# / GPIO101	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO102	SDCM# / GPIO102	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO103	SDCM# / GPIO103	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO104	SDCM# / GPIO104	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO105	SDCM# / GPIO105	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO106	SDCM# / GPIO106	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO107	SDCM# / GPIO107	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO108	SDCM# / GPIO108	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO109	SDCM# / GPIO109	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO110	SDCM# / GPIO110	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO111	SDCM# / GPIO111	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO112	SDCM# / GPIO112	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO113	SDCM# / GPIO113	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO114	SDCM# / GPIO114	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO115	SDCM# / GPIO115	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO116	SDCM# / GPIO116	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO117	SDCM# / GPIO117	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO118	SDCM# / GPIO118	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO119	SDCM# / GPIO119	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO120	SDCM# / GPIO120	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO121	SDCM# / GPIO121	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO122	SDCM# / GPIO122	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO123	SDCM# / GPIO123	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO124	SDCM# / GPIO124	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO125	SDCM# / GPIO125	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO126	SDCM# / GPIO126	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO127	SDCM# / GPIO127	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO128	SDCM# / GPIO128	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO129	SDCM# / GPIO129	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO130	SDCM# / GPIO130	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO131	SDCM# / GPIO131	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO132	SDCM# / GPIO132	98	V <sub>0</sub> , V <sub>5</sub>	IO4	O_SDCM#_R	Native	Native	NA	
GPIO133	SDCM# / GPIO133	98	V <sub>0</sub> , V <sub>5</sub>						





DDRO_DQ[8]	AH40	DQ_9
DDRO_DQ[9]	AH39	DQ_13
DDRO_DQ[13]	AH40	DQ_8
DDRO_DQ[16]	AM38	DQ_17
DDRO_DQ[17]	AM39	DQ_21
DDRO_DQ[21]	AM38	DQ_16
DDRO_DQ[24]	AV37	DQ_25
DDRO_DQ[25]	AW37	DQ_29
DDRO_DQ[29]	AU37	DQ_24
DDRO_DQ[32]	AY6	DQ_33
DDRO_DQ[33]	AU6	DQ_37
DDRO_DQ[37]	AR1	DQ_41
DDRO_DQ[40]	AR4	DQ_45
DDRO_DQ[41]	AR4	DQ_45
DDRO_DQ[45]	AL4	DQ_40
DDRO_DQ[48]	AL4	DQ_43
DDRO_DQ[49]	AL3	DQ_53
DDRO_DQ[53]	AL3	DQ_48
DDRO_DQ[56]	AG1	DQ_57
DDRO_DQ[57]	AG4	DQ_61
DDRO_DQ[61]	AG3	DQ_56
DDRO_DQ[64]	AW33	DQ_65
DDRO_DQ[65]	AV33	DQ_69
DDRO_DQ[69]	AV33	DQ_64

## Bit Swap for layout

6) ECC

SA_CS#11	A9V9	D8_SCS_A#1	(15)
SA_CS#22	AU10	D8_SCS_A#2	(16)
SA_CS#55	AW8	D8_SCS_A#3	(16)
SA_CLK[0]	AY15	D8_MA_CLK0	(15)
SA_CLK#10	AY16	D8_MA_CLK#0	(15)
SA_CLK#11	AW15	D8_MA_CLK#1	(15)
SA_CLK#12	AV15		

1 OF 10

CH3  
0.1uF  
Dummy  
16V, X7R, +/-10%



Title

**CPU-1: DDR3\_CHA**

DWG NO
--------

## Amazon SFF

Rev **A00**

Date: Tuesday, March 12, 2013

Sheet 9 of 66

# DDR3 CH-B

(17,18) D3\_DQ\_B[63..0] <<<

UH1B

D3_DQ_B0	AE34	SB_DQ[0]
D3_DQ_B1	AE35	SB_DQ[1]
D3_DQ_B2	AG35	SB_DQ[2]
D3_DQ_B3	AH35	SB_DQ[3]
D3_DQ_B4	AD34	SB_DQ[4]
D3_DQ_B5	AD35	SB_DQ[5]
D3_DQ_B6	AG34	SB_DQ[6]
D3_DQ_B7	AH34	SB_DQ[7]
D3_DQ_B8	AL34	SB_DQ[8]
D3_DQ_B9	AK35	SB_DQ[9]
D3_DQ_B10	AK31	SB_DQ[10]
D3_DQ_B11	AL31	SB_DQ[11]
D3_DQ_B12	AK34	SB_DQ[12]
D3_DQ_B13	AK35	SB_DQ[13]
D3_DQ_B14	AK32	SB_DQ[14]
D3_DQ_B15	AL32	SB_DQ[15]
D3_DQ_B17	AP34	SB_DQ[16]
D3_DQ_B19	AN31	SB_DQ[17]
D3_DQ_B23	AP31	SB_DQ[18]
D3_DQ_B20	AN35	SB_DQ[19]
D3_DQ_B16	AP35	SB_DQ[21]
D3_DQ_B18	AN32	SB_DQ[22]
D3_DQ_B22	AP32	SB_DQ[23]
D3_DQ_B25	AM29	SB_DQ[24]
D3_DQ_B28	AM28	SB_DQ[25]
D3_DQ_B27	AR29	SB_DQ[26]
D3_DQ_B30	AR28	SB_DQ[27]
D3_DQ_B24	AL29	SB_DQ[28]
D3_DQ_B29	AL28	SB_DQ[29]
D3_DQ_B31	AP28	SB_DQ[30]
D3_DQ_B32	AR12	SB_DQ[31]
D3_DQ_B33	AP12	SB_DQ[32]
D3_DQ_B34	AL13	SB_DQ[33]
D3_DQ_B35	AL12	SB_DQ[34]
D3_DQ_B36	AR13	SB_DQ[35]
D3_DQ_B37	AP13	SB_DQ[36]
D3_DQ_B38	AM13	SB_DQ[37]
D3_DQ_B39	AM12	SB_DQ[38]
D3_DQ_B45	AR9	SB_DQ[39]
D3_DQ_B41	AP9	SB_DQ[40]
D3_DQ_B47	AR6	SB_DQ[41]
D3_DQ_B43	AP6	SB_DQ[42]
D3_DQ_B44	AR10	SB_DQ[43]
D3_DQ_B40	AP10	SB_DQ[44]
D3_DQ_B46	AR7	SB_DQ[45]
D3_DQ_B42	AP7	SB_DQ[46]
D3_DQ_B52	AM9	SB_DQ[47]
D3_DQ_B53	AL9	SB_DQ[48]
D3_DQ_B50	AL6	SB_DQ[49]
D3_DQ_B55	AL7	SB_DQ[50]
D3_DQ_B48	AM10	SB_DQ[51]
D3_DQ_B49	AL10	SB_DQ[52]
D3_DQ_B54	AM6	SB_DQ[53]
D3_DQ_B51	AM7	SB_DQ[54]
D3_DQ_B61	AH6	SB_DQ[55]
D3_DQ_B60	AH7	SB_DQ[56]
D3_DQ_B59	AE6	SB_DQ[57]
D3_DQ_B63	AE7	SB_DQ[58]
D3_DQ_B56	AJ6	SB_DQ[59]
D3_DQ_B57	AJ7	SB_DQ[60]
D3_DQ_B58	AF6	SB_DQ[61]
D3_DQ_B62	AF7	SB_DQ[62]
	AF35	SB_DQ[63]
(17,18) D3_DQS_B0	AL33	SB_DQS[0]
(17,18) D3_DQS_B1	AP33	SB_DQS[1]
(17,18) D3_DQS_B2	AN28	SB_DQS[2]
(17,18) D3_DQS_B3	AN12	SB_DQS[3]
(17,18) D3_DQS_B4	AP8	SB_DQS[4]
(17,18) D3_DQS_B5	AL8	SB_DQS[5]
(17,18) D3_DQS_B6	AG7	SB_DQS[6]
(17,18) D3_DQS_B7	AN25	SB_DQS[7]
(17,18) D3_DQS_B8	AK33	SB_DQS[8]
(17,18) D3_DQS_B#0	AF34	SB_DQS[9]
(17,18) D3_DQS_B#1	AN33	SB_DQS[10]
(17,18) D3_DQS_B#2	AN29	SB_DQS[11]
(17,18) D3_DQS_B#3	AN13	SB_DQS[12]
(17,18) D3_DQS_B#4	AR8	SB_DQS[13]
(17,18) D3_DQS_B#5	AM8	SB_DQS[14]
(17,18) D3_DQS_B#6	AG6	SB_DQS[15]
(17,18) D3_DQS_B#7	AN26	SB_DQS[16]
(17,18) D3_DQS_B#8		SB_DQS[17]

SB_MA[0]	AL19	D3_MAB0
SB_MA[1]	AK23	D3_MAB1
SB_MA[2]	AM22	D3_MAB2
SB_MA[3]	AM23	D3_MAB3
SB_MA[4]	AP23	D3_MAB4
SB_MA[5]	AL23	D3_MAB5
SB_MA[6]	AY24	D3_MAB6
SB_MA[7]	AV25	D3_MAB7
SB_MA[8]	AU26	D3_MAB8
SB_MA[9]	AW25	D3_MAB9
SB_MA[10]	AP18	D3_MAB10
SB_MA[11]	AY25	D3_MAB11
SB_MA[12]	AV26	D3_MAB12
SB_MA[13]	AR15	D3_MAB13
SB_MA[14]	AV27	D3_MAB14
SB_MA[15]	AY28	D3_MAB15
SB_ODT[0]	AM17	
SB_ODT[1]	AL16	
SB_ODT[2]	AM16	
SB_ODT[3]	AK15	
SB_ECC_CB[0]	AM26	
SB_ECC_CB[1]	AM25	
SB_ECC_CB[2]	AP25	
SB_ECC_CB[3]	AP26	
SB_ECC_CB[4]	AL26	
SB_ECC_CB[5]	AL25	
SB_ECC_CB[6]	AR26	
SB_ECC_CB[7]	AR25	
SB_BS[0]	AK17	D3_BAB0
SB_BS[1]	AL18	D3_BAB1
SB_BS[2]	AW28	D3_BAB2
SB_CKE[0]	AW29	
SB_CKE[1]	AY29	
SB_CKE[2]	AU28	
SB_CKE[3]	AU29	
SB_CS[0]	AP17	
SB_CS[1]	AN15	
SB_CS[2]	AN17	
SB_CS[3]	AL15	
SB_CLK[0]	AN20	
SB_CLK[1]	AM21	
SB_CLK[2]	AP22	
SB_CLK[3]	AP21	
SB_CK[0]	AN20	
SB_CK[1]	AN21	
SB_CK[2]	AP19	
SB_CK[3]	AP20	
SB_CAS#	AP16	
RSVD_49	AL20	
SB_RAS#	AM18	
SB_WE#	AK16	
SA_DIMM_VREFDQ	AB39	H CPU DIMM VREF A
SB_DIMM_VREFDQ	AB40	H CPU DIMM VREF B

D3\_MAB[15..0] (17,18)

D3\_ODT\_B0 (17)  
D3\_ODT\_B1 (17)  
D3\_ODT\_B2 (18)  
D3\_ODT\_B3 (18)

D3\_SB\_ECC\_CB4 (17,18)  
D3\_SB\_ECC\_CB5 (17,18)  
D3\_SB\_ECC\_CB6 (17,18)  
D3\_SB\_ECC\_CB7 (17,18)  
D3\_SB\_ECC\_CB8 (17,18)  
D3\_SB\_ECC\_CB1 (17,18)  
D3\_SB\_ECC\_CB2 (17,18)  
D3\_SB\_ECC\_CB3 (17,18)  
D3\_BAB[2..0] (17,18)

D3\_CKE\_B0 (17)  
D3\_CKE\_B1 (17)  
D3\_CKE\_B2 (18)  
D3\_CKE\_B3 (18)

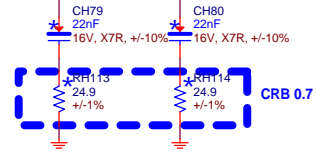
D3\_SCB\_B#0 (17)  
D3\_SCB\_B#1 (17)  
D3\_SCB\_B#2 (18)  
D3\_SCB\_B#3 (18)

D3\_MB\_CLK0 (17)  
D3\_MB\_CLK#0 (17)  
D3\_MB\_CLK1 (17)  
D3\_MB\_CLK#1 (17)

D3\_MB\_CLK2 (18)  
D3\_MB\_CLK#2 (18)  
D3\_MB\_CLK3 (18)  
D3\_MB\_CLK#3 (18)

D3\_CASB# (17,18)  
D3\_RASB# (17,18)  
D3\_WEB# (17,18)

H\_CPU\_DIMM\_VREF\_A (15)  
H\_CPU\_DIMM\_VREF\_B (17)



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PE115027-4041-0DF



Title  
**CPU-2: DDR3\_CHB**

DWG NO  
**Amazon SFF**

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## UH1E



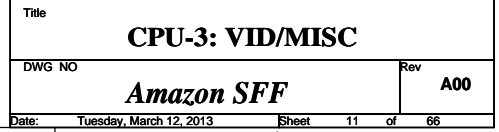
+1P05V\_PCH

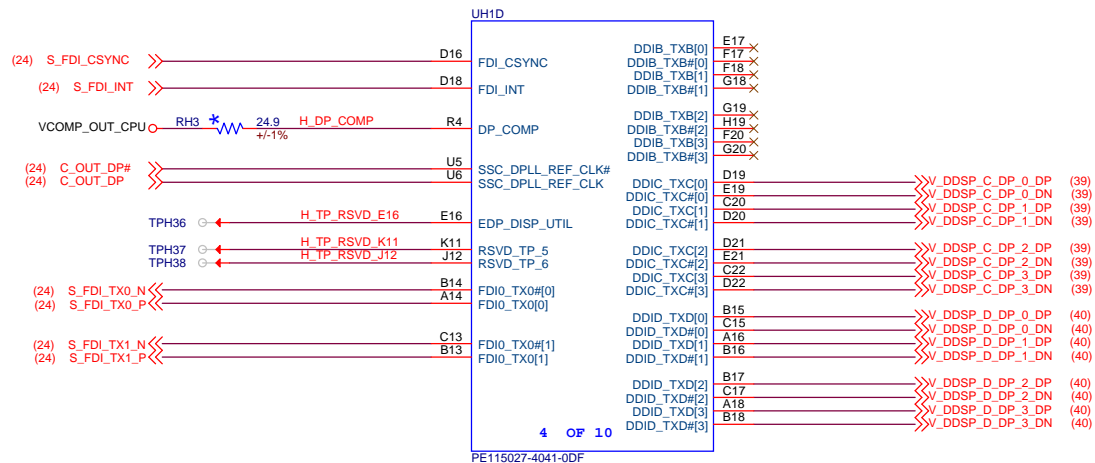
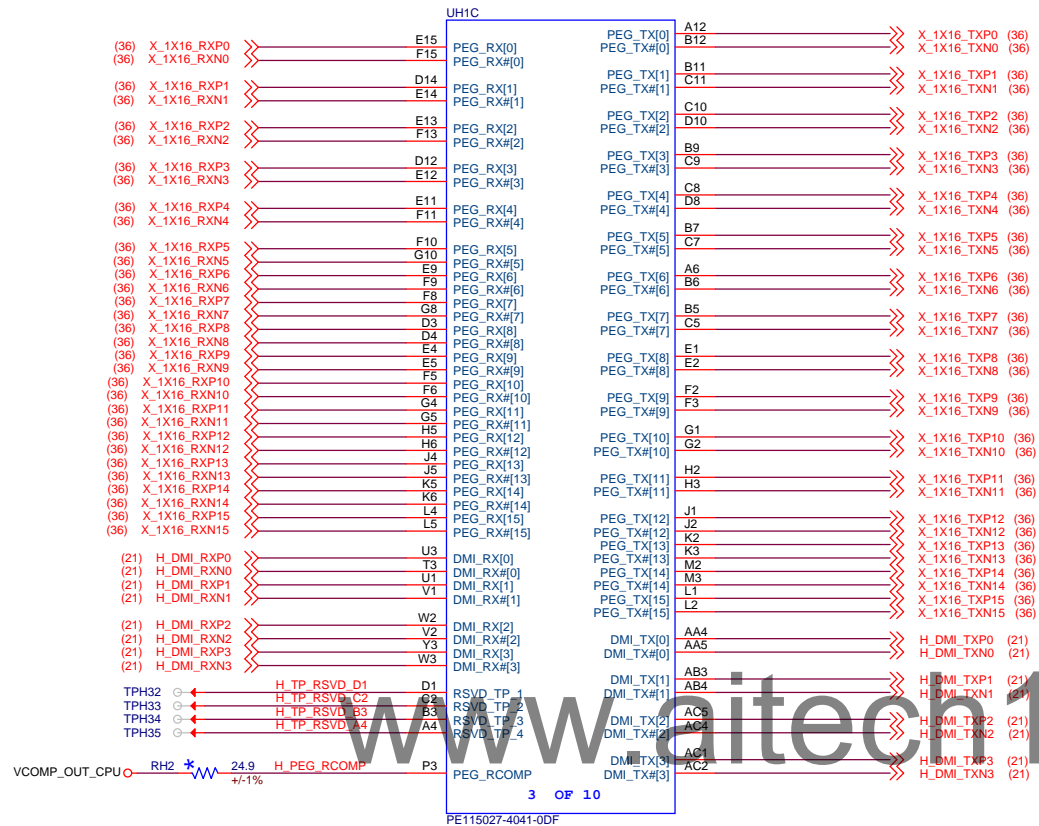
20120326: RH72, RH9 pull-up to +1P05V\_PCH  
20120413: RH18 change to 1k and stuffed, follow CRB1.0

+3V\_S5

H\_CPU\_VCCIO\_RIGHT

20120413: Delete RH57, CH39 and add TPH41, follow CRB1.0

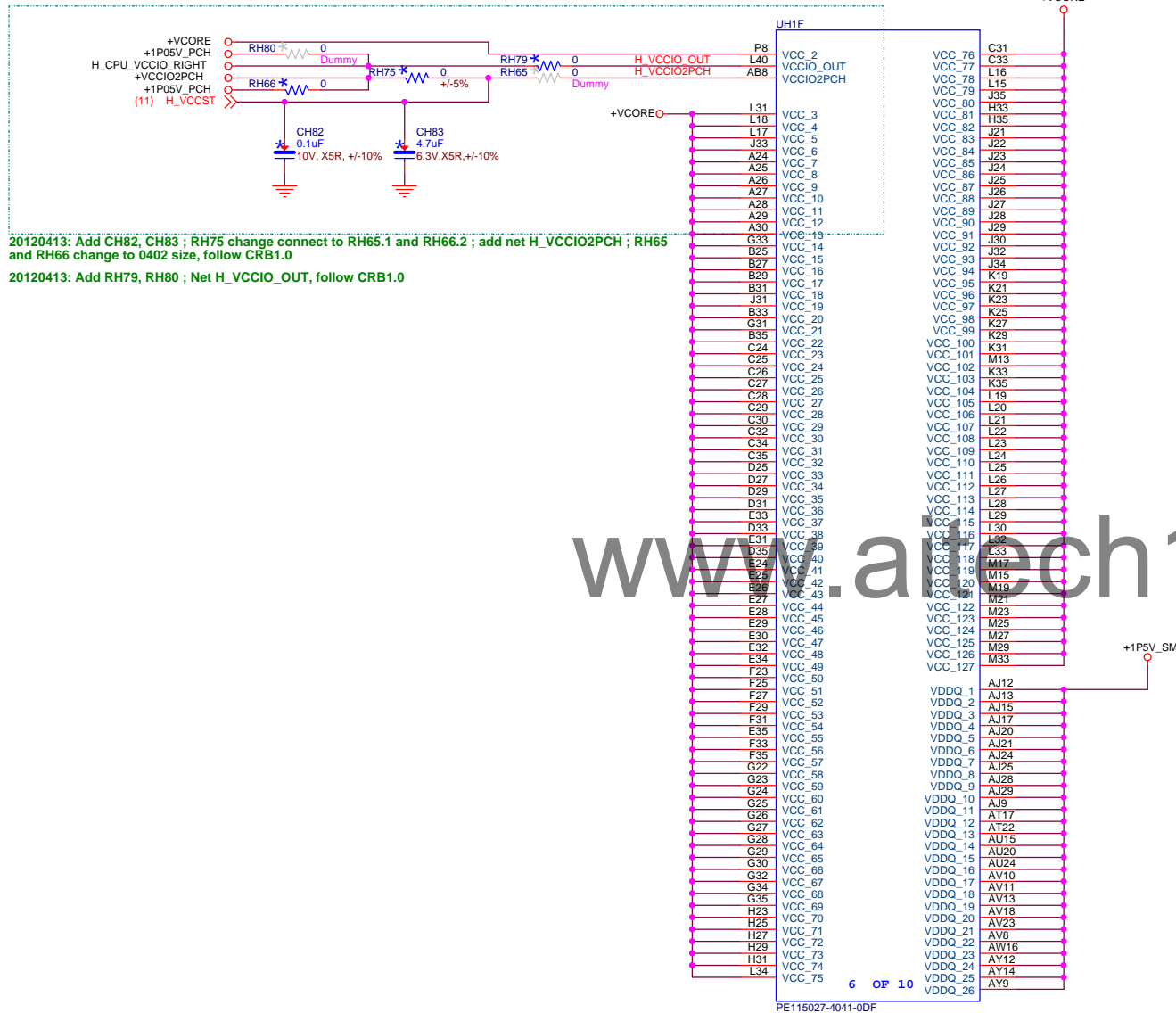


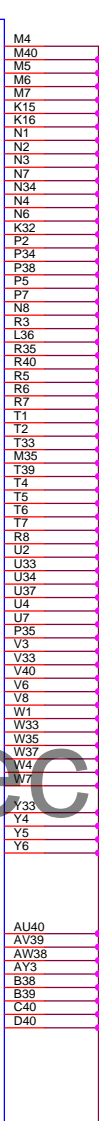
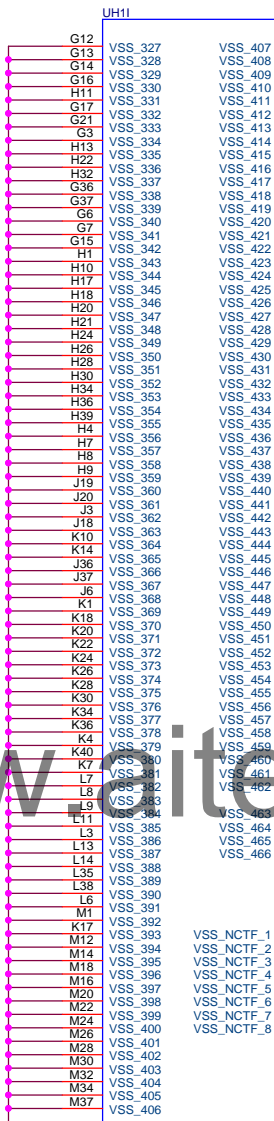
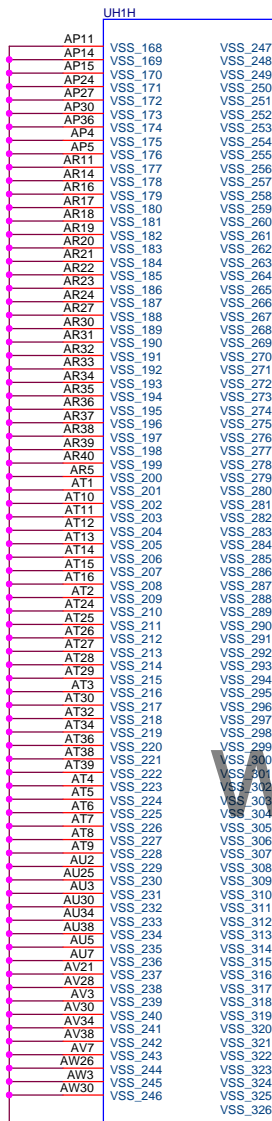
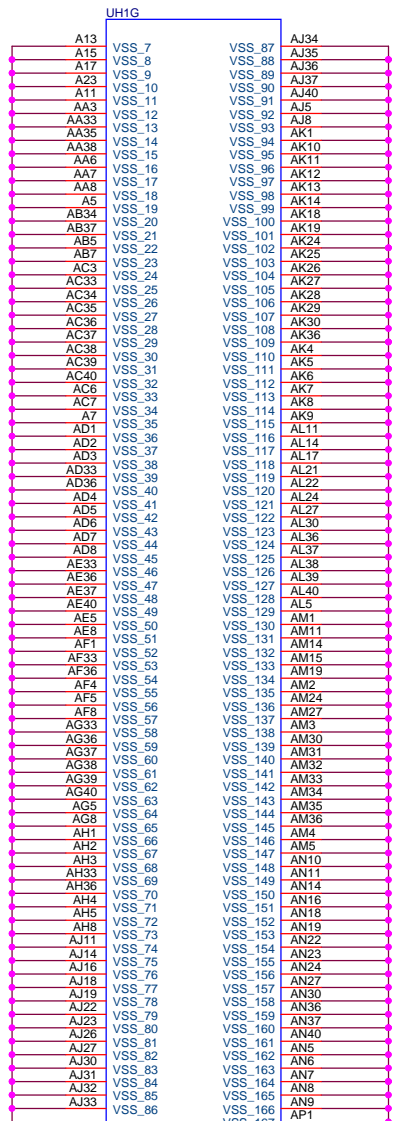


Display Port1

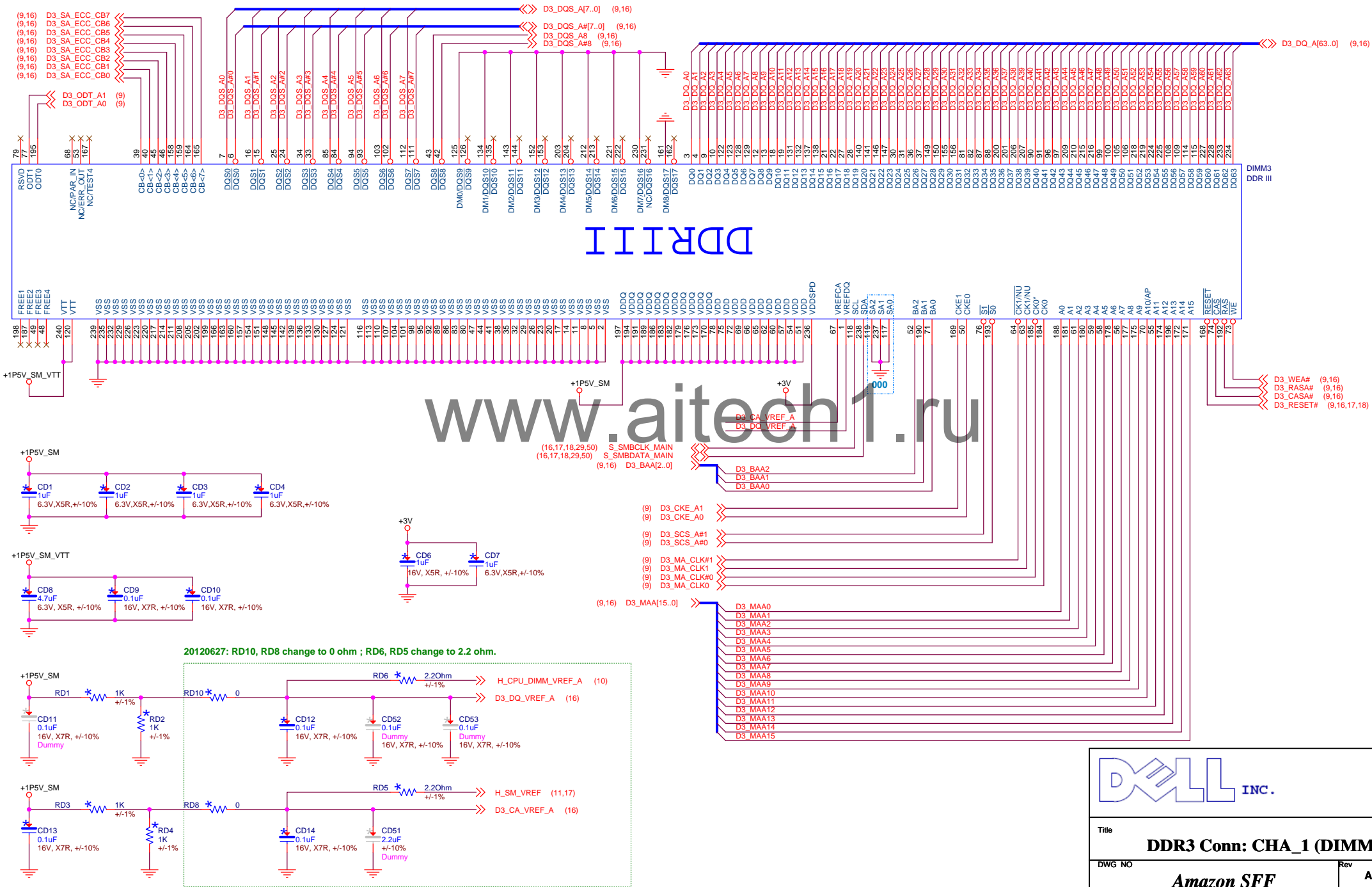
Display Port2







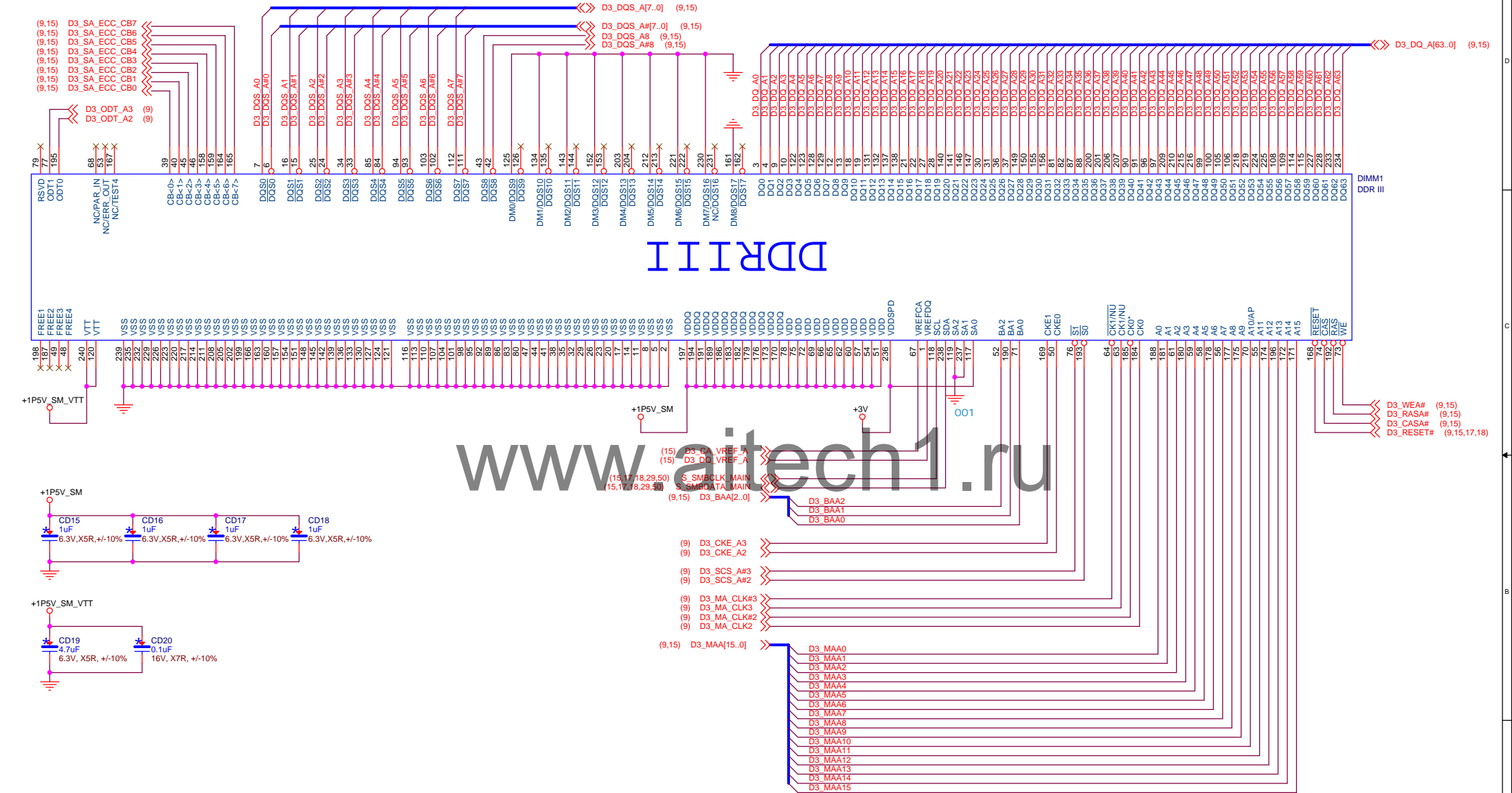




Title	<b>DDR3 Conn: CHA_1 (DIMM3)</b>
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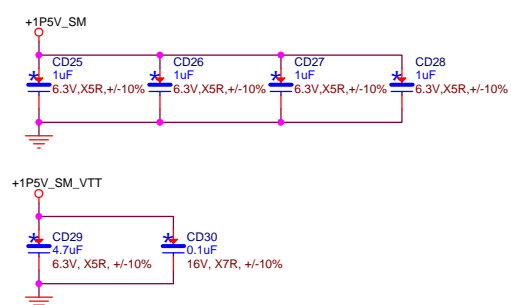
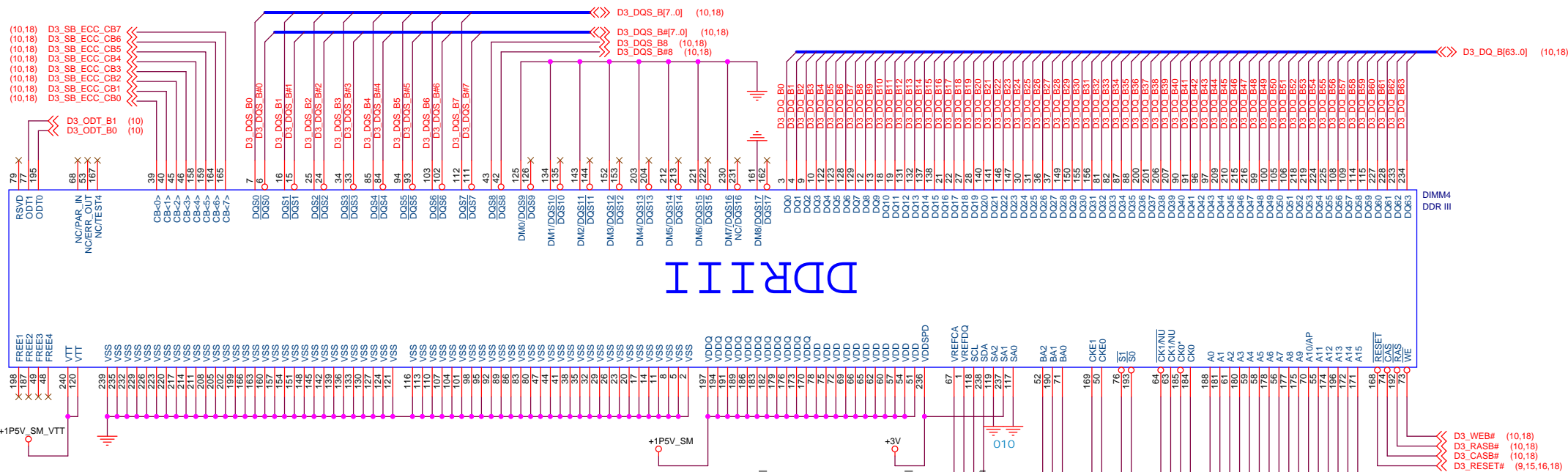
DWG NO	Rev
<i>Amazon SFF</i>	A00



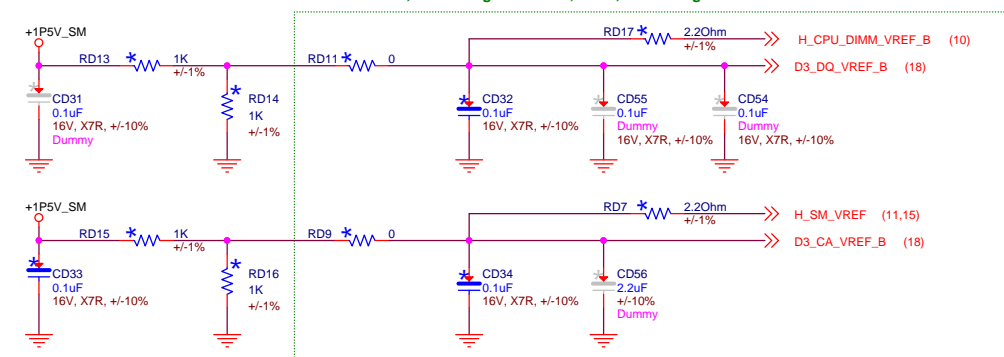


Title **DDR3 Conn: CHA\_2 (DIMM1)**

DWG NO	Rev
<i>Amazon SFF</i>	A00

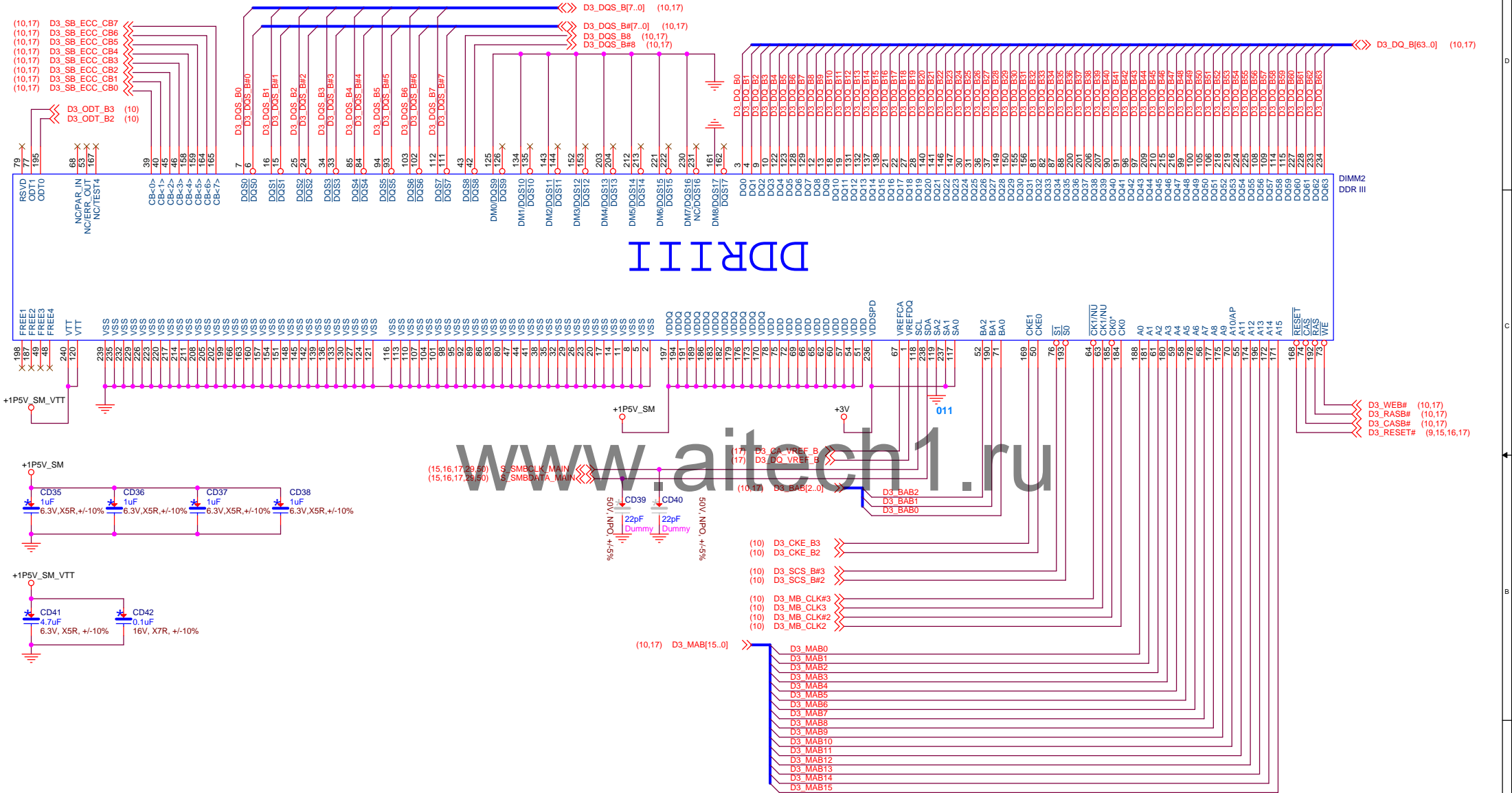


20120627: RD11, RD9 change to 0 ohm ; RD17, RD7 change to 2.2 ohm.



Title	<b>DDR3 Conn: CHB_1 (DIMM4)</b>
-------	---------------------------------

DWG NO	Rev
<i>Amazon SFF</i>	A00



Title

DDR3 Conn: CHB\_2 (DIMM2)

DWG NO

Amazon SFF

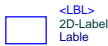
Rev

A00

Date: Tuesday, March 12, 2013

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2D LABEL



ME\_PAD



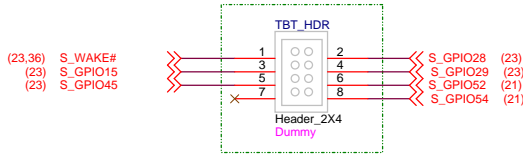
20120412: Add for ME request  
20120628: Delete ME\_PAD for ME suggestion

www.aitech1.ru



Title			LABEL		
DWG NO		Rev			A00
Date: Tuesday, March 12, 2013		Sheet 19 of 66			

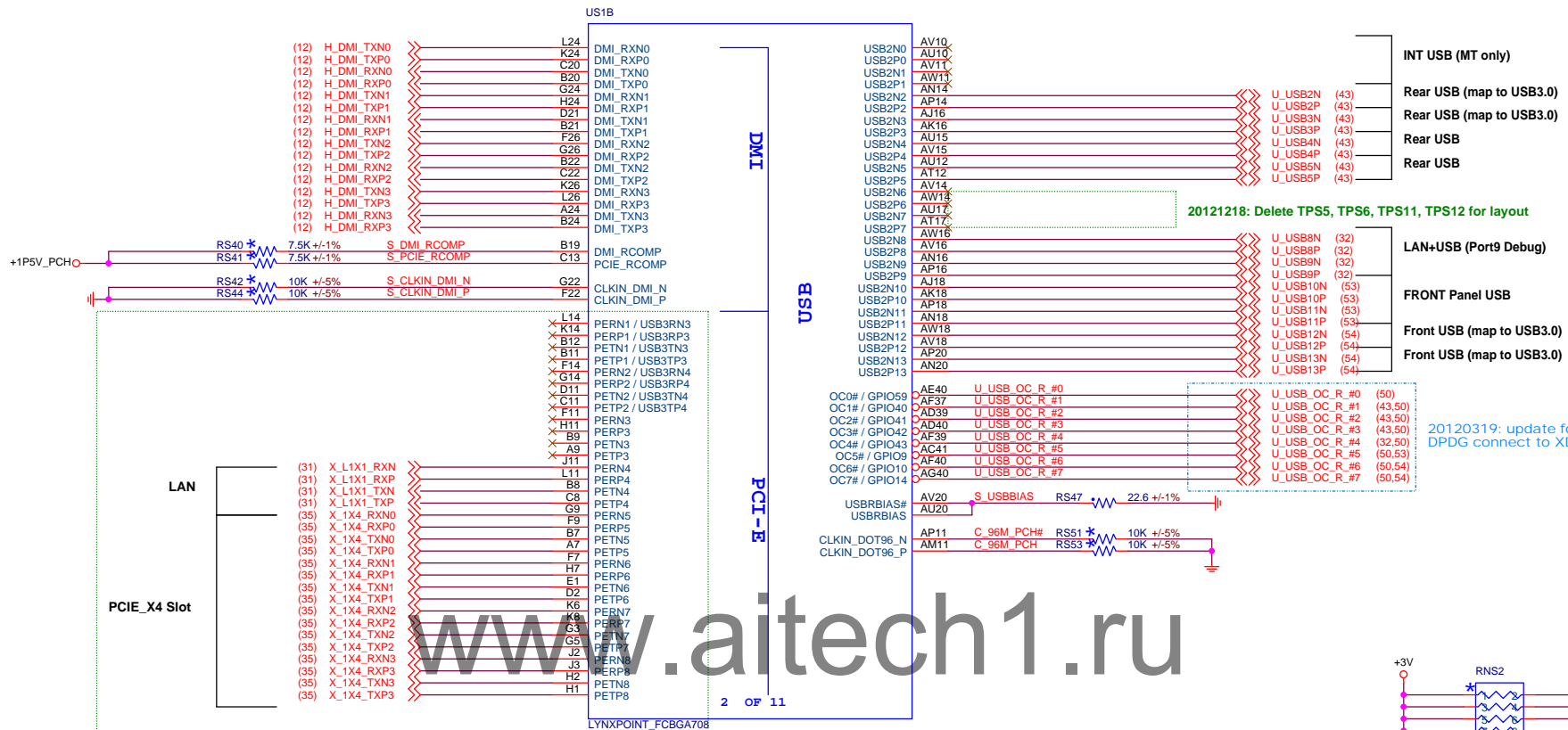
20120626: Add TBT\_HDR  
20120703: TBT\_HDR compoment REMARK cahnge to Remark  
20120716: TBT\_HDR stuffed.  
20120828: TBT\_HDR Dummy by Dell



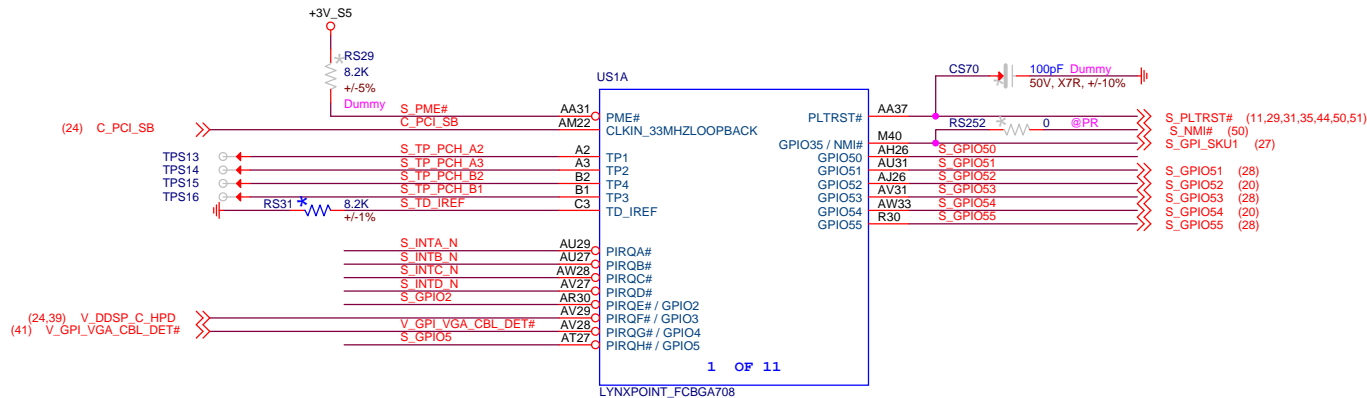
www.aitech1.ru



Title			TBT_HDR		
DWG NO			Amazon SFF		
Date: Tuesday, March 12, 2013			Sheet 20 of 66		
			Rev A00		



20120611: PCIe porting SWAP, LAN change to port-4 ; PCIe4 change to port-5 - port-8 ; Delete TPS44, TPS45, TPS46, TPS47, TPS48, TPS49, TPS50, TPS51



INT USB (MT only)  
Rear USB (map to USB3.0)  
Rear USB (map to USB3.0)  
Rear USB  
Rear USB

LAN+USB (Port9 Debug)

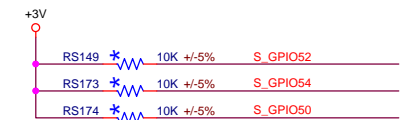
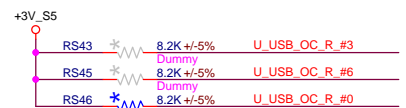
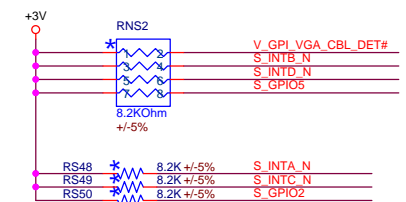
FRONT Panel USB

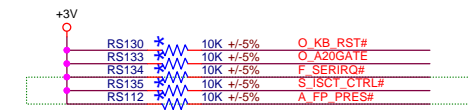
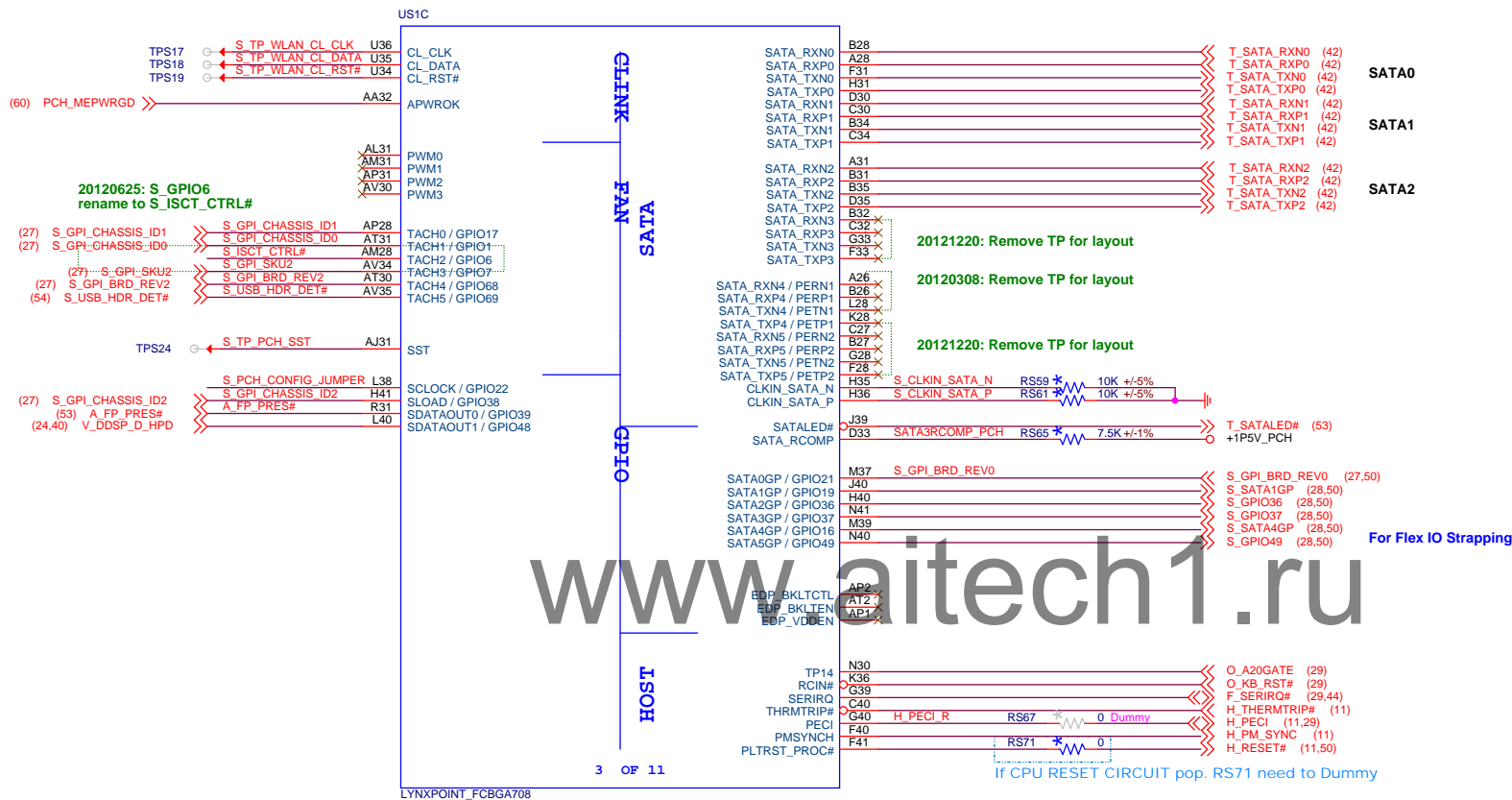
Front USB (map to USB3.0)

Front USB (map to USB3.0)

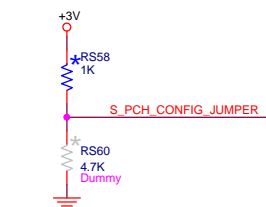
20121218: Delete TPSS, TPS6, TPS11, TPS12 for layout

20120319: update for follow Intel DPDG connect to XDP\_PCH

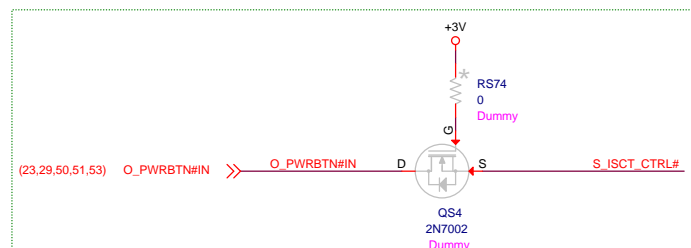




20120625: S\_GPIO6  
rename to S\_ISCT\_CTRL#



20120625: Add QS4 and S\_ISCT\_CTRL#  
20120627: Dummy QS4  
20120911: QS4.G change to +3V from +5V  
20120911: Add RS74 connect +3V to QS4



**DELL INC.**

Title  
**PCH-2: SATA/HOST/GPIO**

DWG NO  
**Amazon SFF**

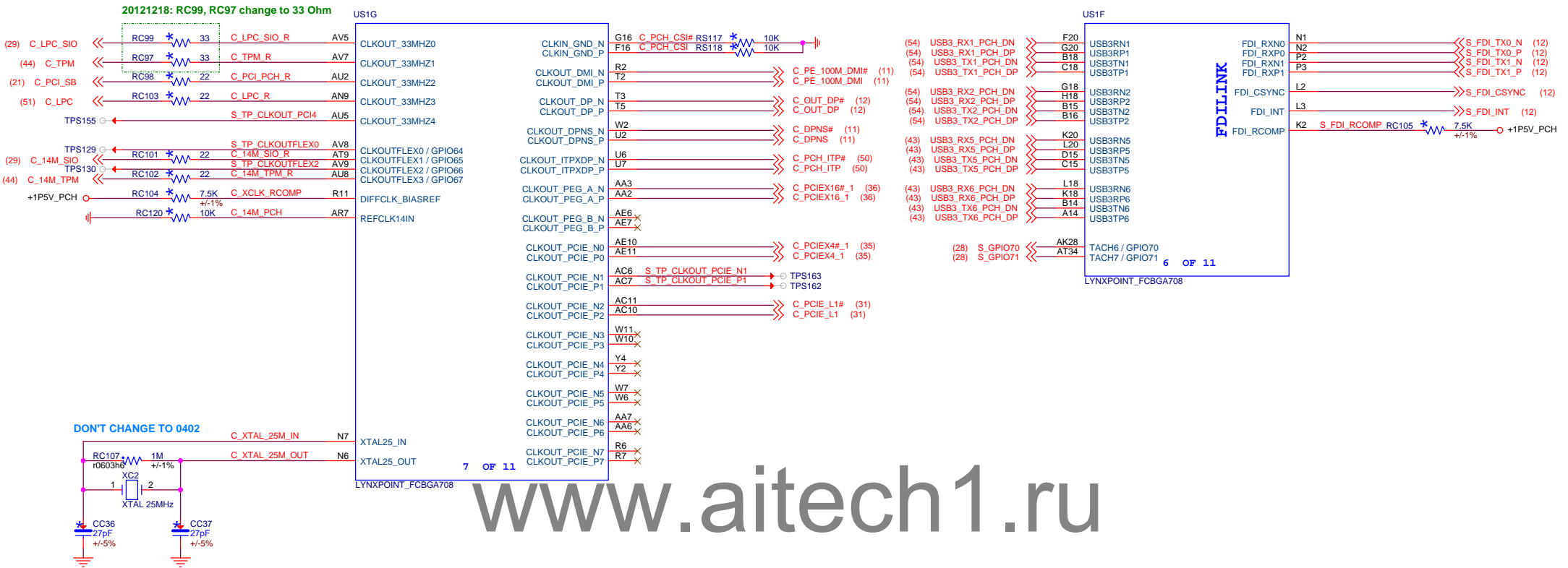
Rev  
**A00**

Date: Tuesday, March 12, 2013 Sheet 22 of 66

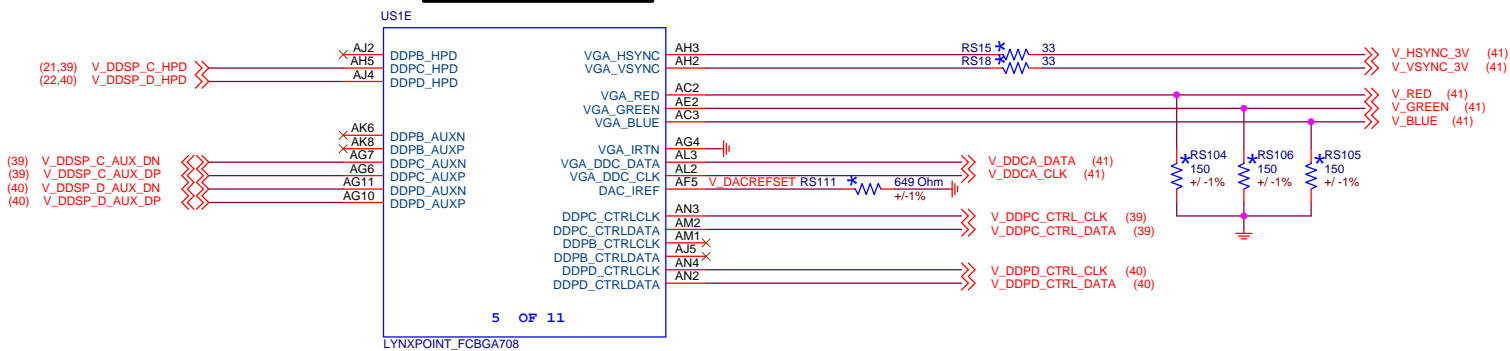


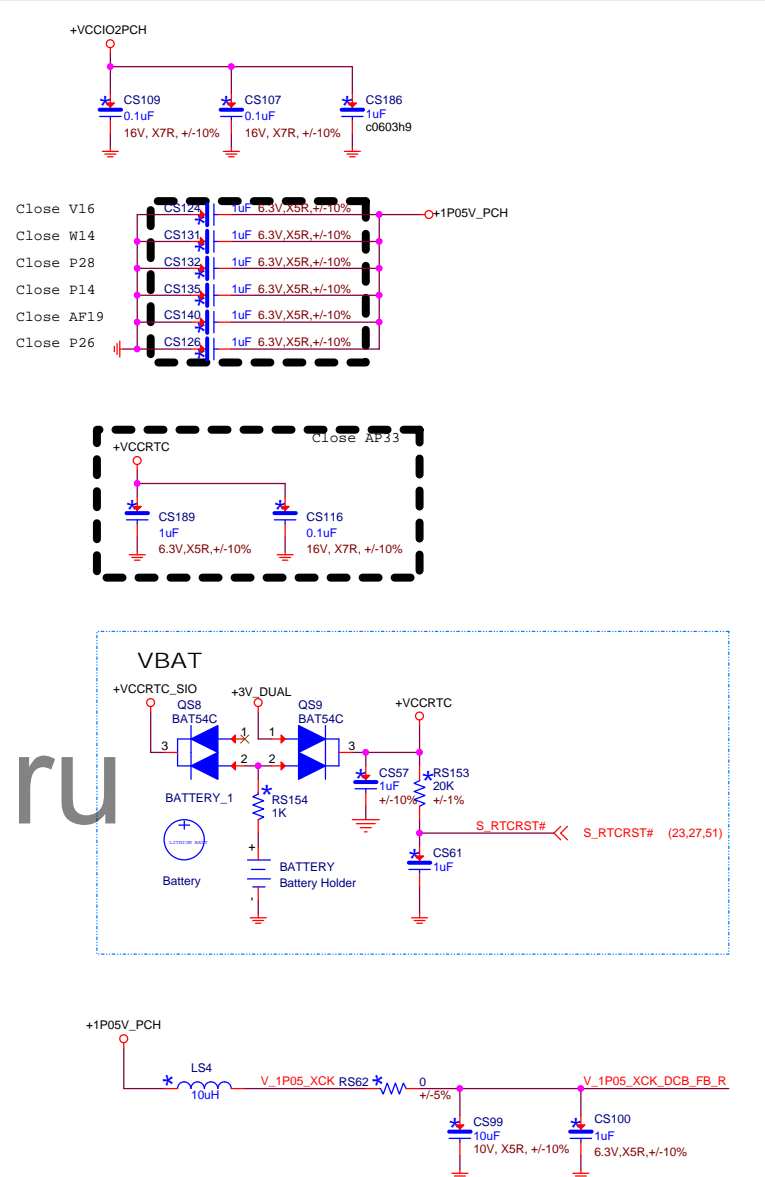
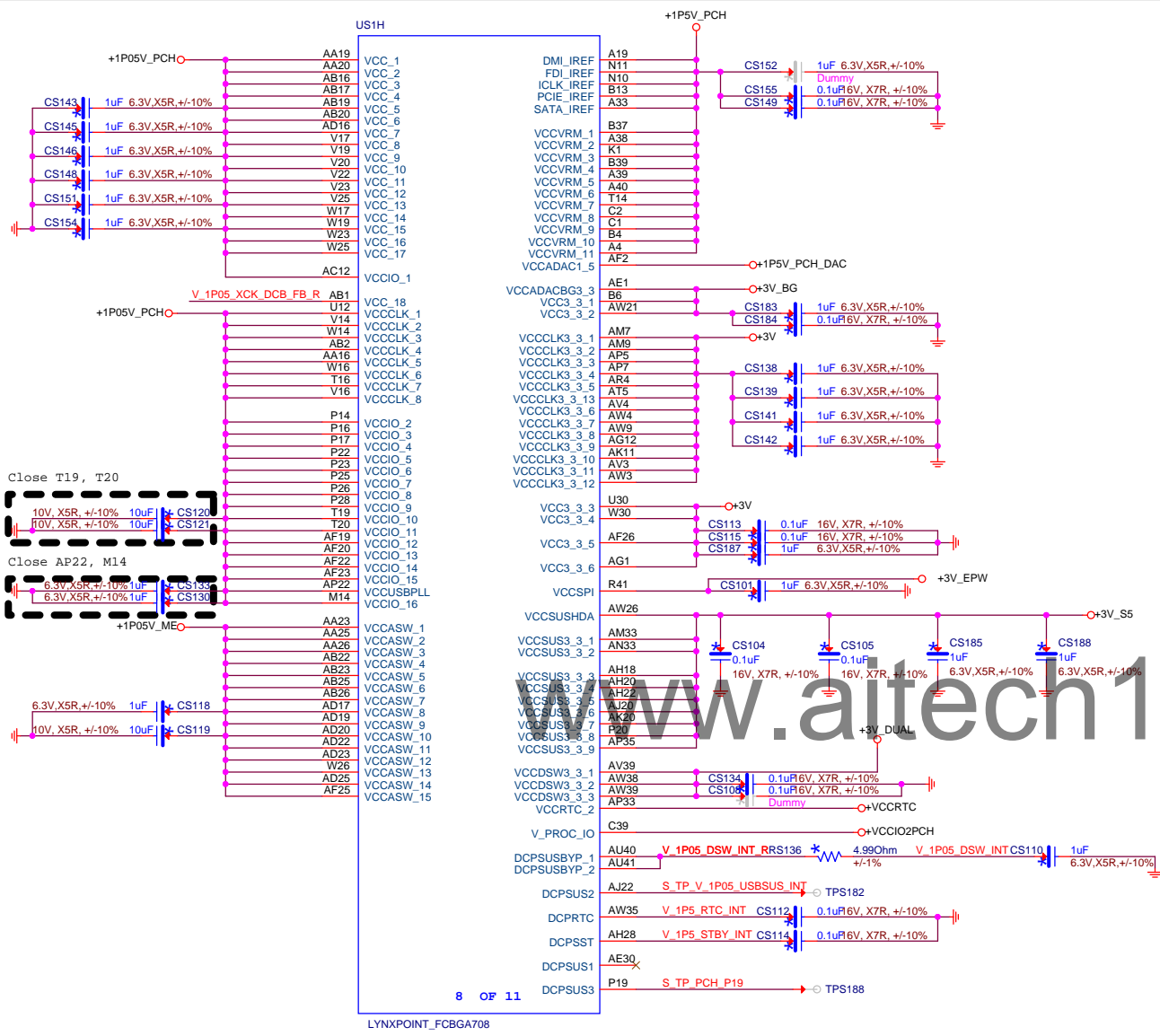


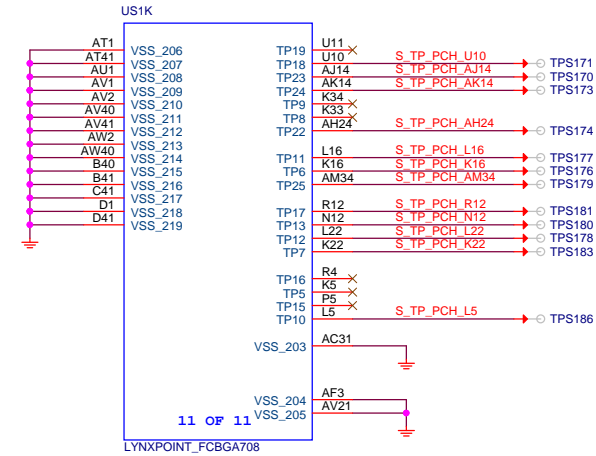
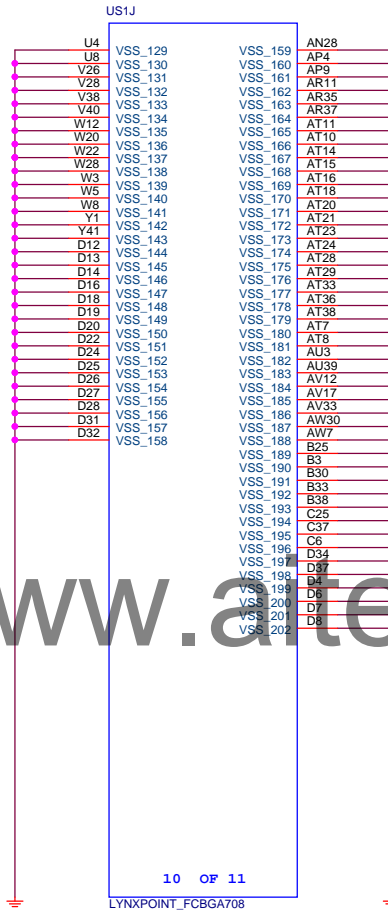
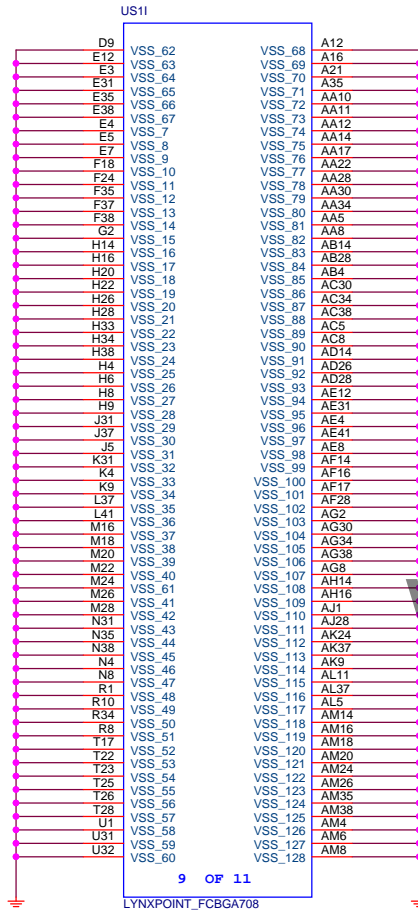
## PCH - CLOCK DISTRIBUTION



## PCH - DP AND RGB

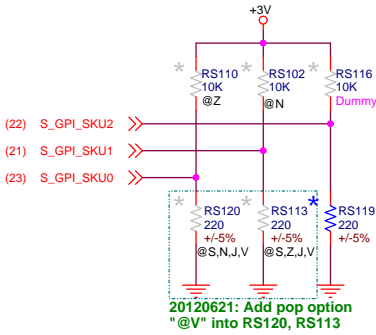






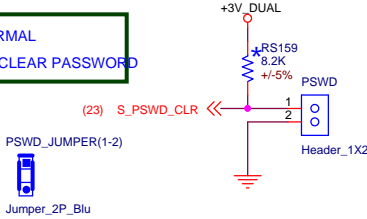
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

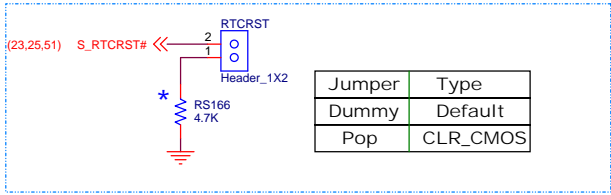


Clear Password

1-2: NORMAL  
EMPTY: CLEAR PASSWORD



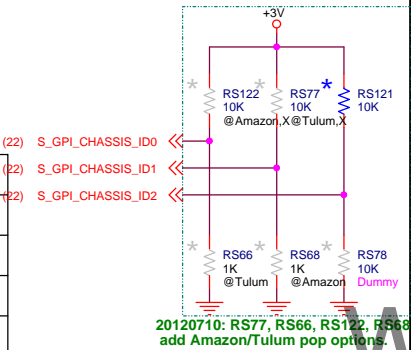
CLR\_CMOS



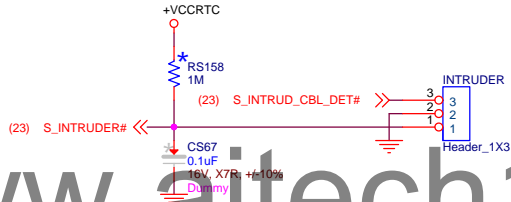
Jumper	Type
Dummy	Default
Pop	CLR_CMOS

Chassis ID

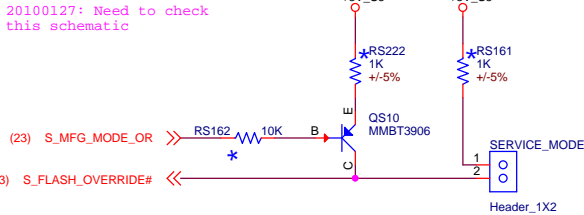
ID2	ID1	ID0	Type
1	0	1	SFF
1	1	0	Tulum SFF
1	1	1	X-SFF
0	0	0	MT
1	0	0	Tulum MT
0	1	0	X-MT
0	1	1	USFF



Chassis Intruder

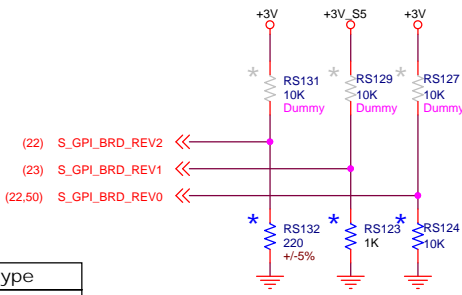


ME Disable (Flash override)

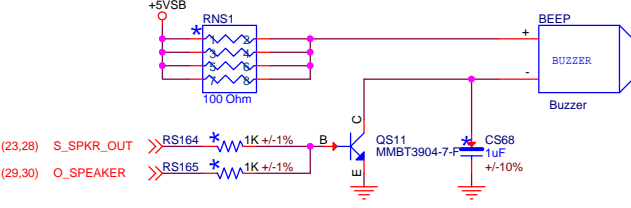


BOARD ID

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



BEEP

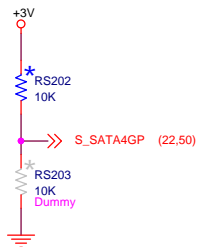


PCH HeatSink

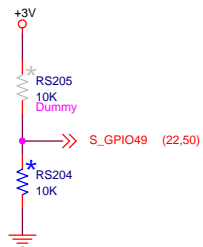


Title		
PCH-8: MISC CONN/BEEP/ID		
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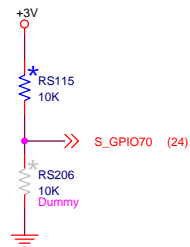
GPIO16 (H-&gt;SATA4 ; L-&gt;PCle1)



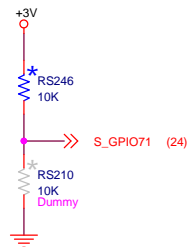
GPIO49 (H-&gt;SATA5 ; L-&gt;PCle2)



GPIO70 (H-&gt;PCle1 ; L-&gt;USB3 3)

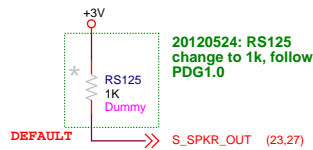


GPIO71 (H-&gt;PCle2 ; L-&gt;USB3 4)



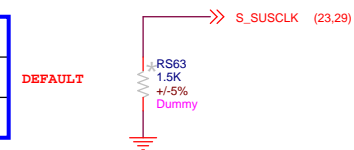
No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



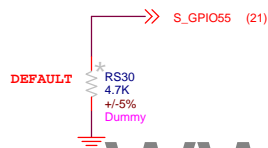
On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.



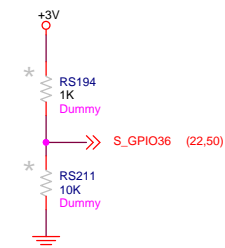
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



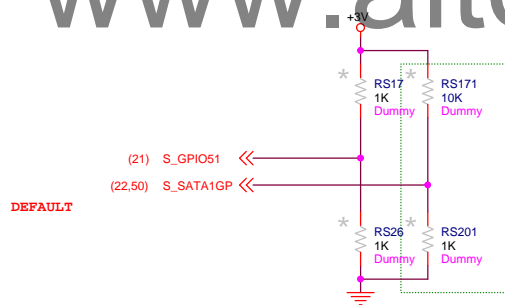
DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage

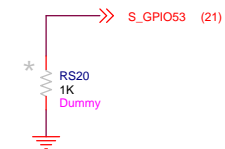


Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

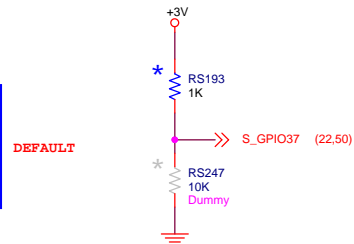


DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW



TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality



Title

PCH-9: STRAP OPTION

DWG NO

Amazon SFF

Rev

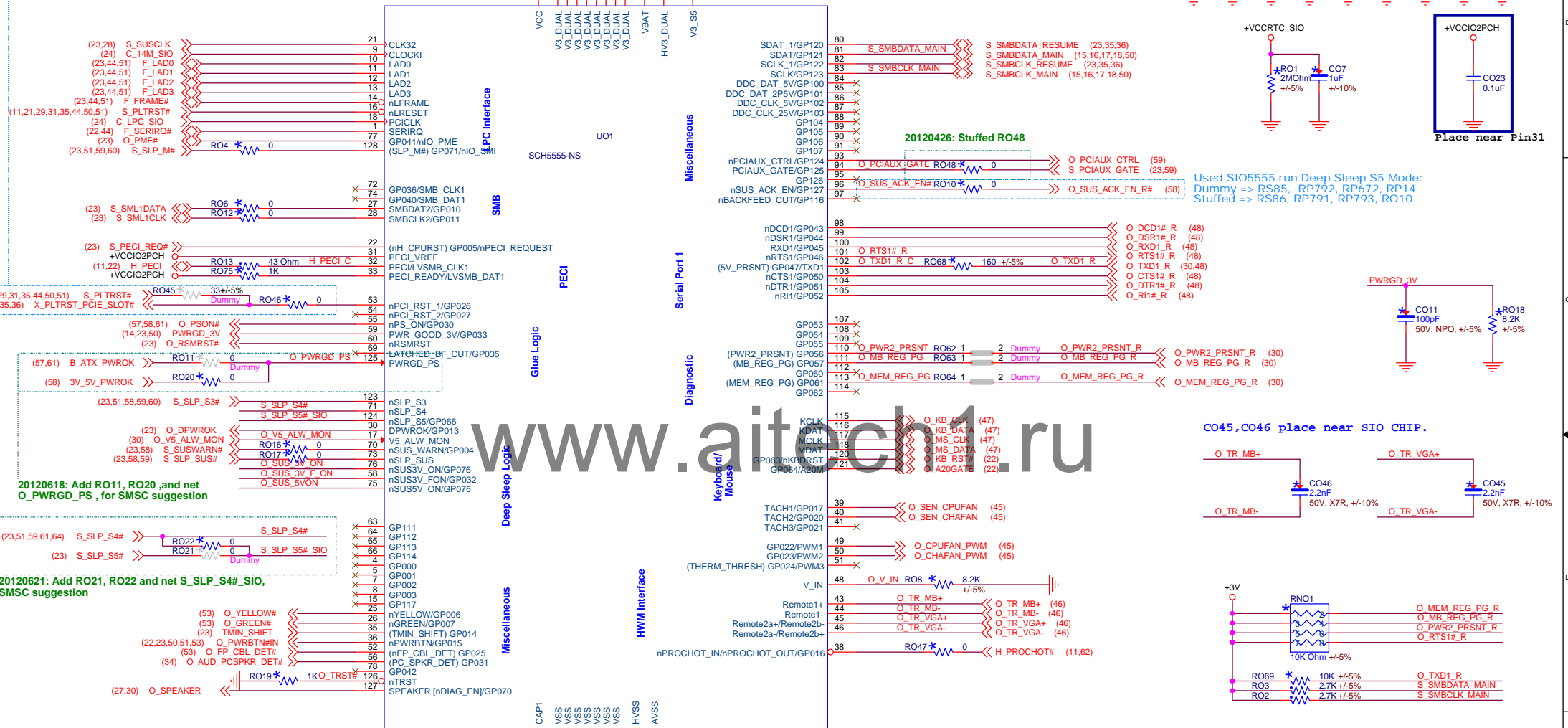
A00

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20120502: UO1 change to SCH555-NS\_B, version B.



The schematic diagram illustrates the power supply section of the ADXL05 demo board. It features a +3V DUAL input connected to a network of resistors (RO41, RO42, RO43, RO44), capacitors (CO15, CO30), and a diode (DO1 SD103AW). The output is labeled O\_SUS\_3V\_ON and O\_SUS\_5V\_ON.

- Inputs:** +3V DUAL, O\_SUS\_3V\_ON, O\_SUS\_5V\_ON, +5VSB.
- Resistors:** RO41 (47K), RO42 (220), RO43 (15K), RO44 (22K).
- Capacitors:** CO15 (1uF), CO30 (2.2uF, +/-10%).
- Diode:** DO1 SD103AW.

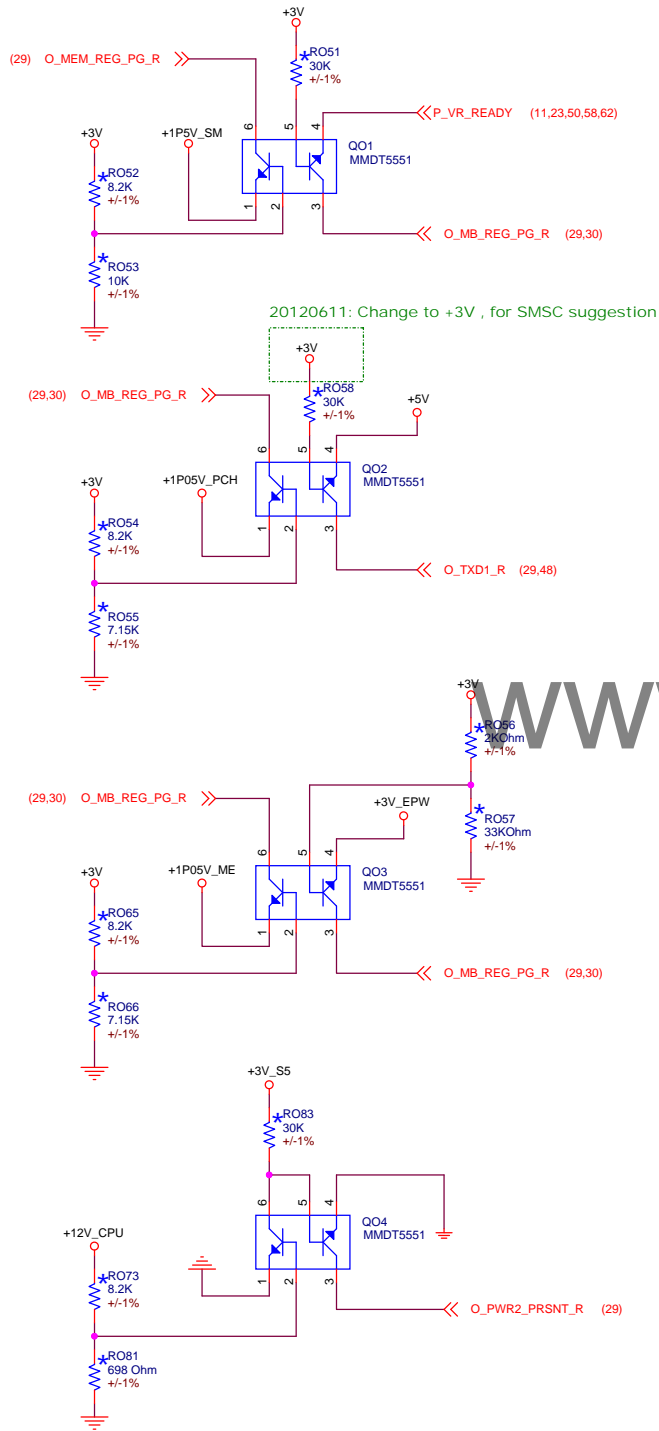
A circuit diagram showing a connection from a pin labeled **H\_PEC1\_C** to a capacitor labeled **CO10 0.1uF Dummy**. The capacitor is connected to ground, represented by a standard ground symbol.



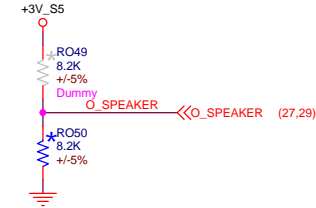
Title		<b>SIO-SCH5555-1</b>	
DWG NO	<i>Amazon SFF</i>	Rev	<b>A00</b>
Date:	Tuesday, March 12, 2013	Sheet	29 of 66



# 5555 PRE-POST DIAG Monitor



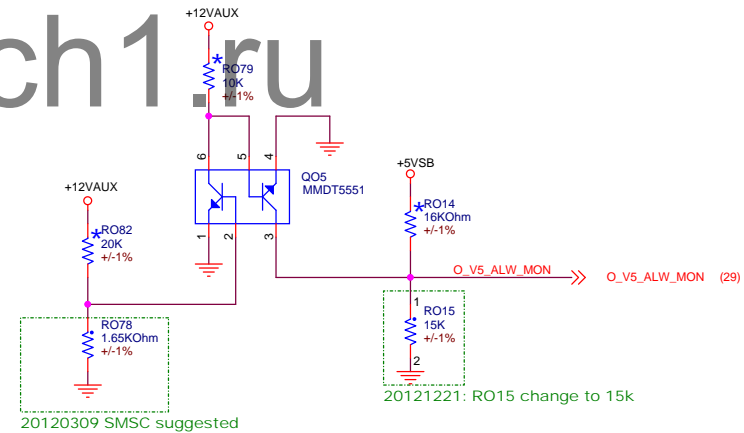
# SIO STRAPING



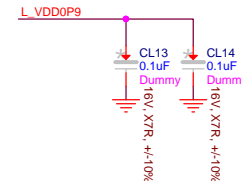
SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

# SIO5555 V5\_ALW Monitor



## Intel Clarkville

[illegible][illegible]**LAN: Intel Clarkville**

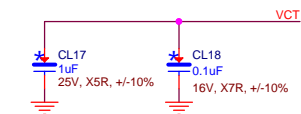
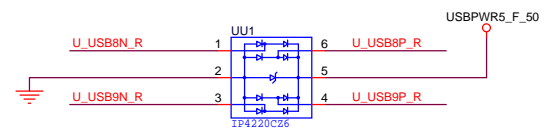
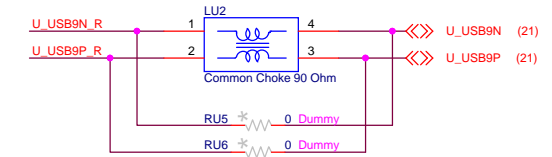
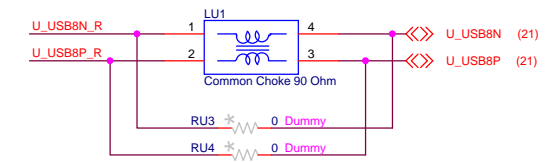
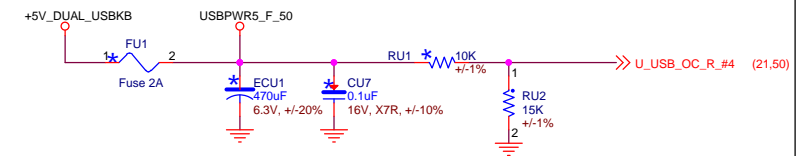
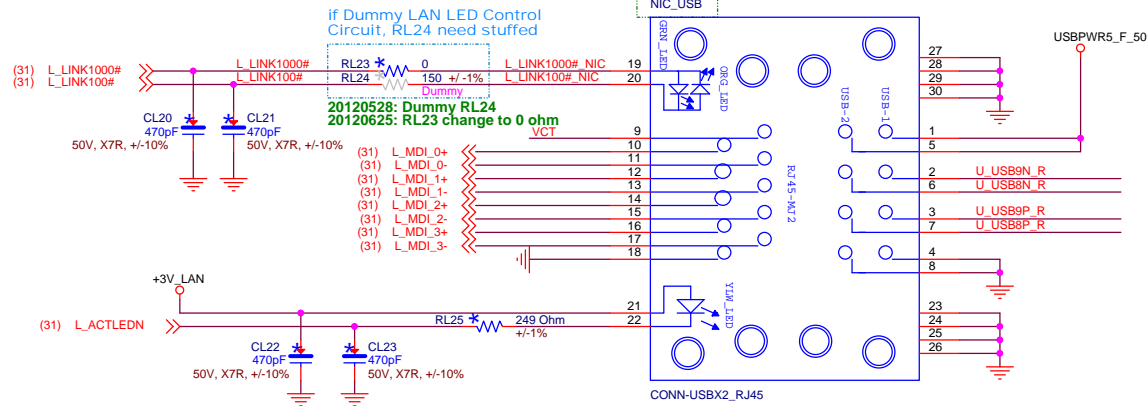
## Amazon SFF

Rev **A00**

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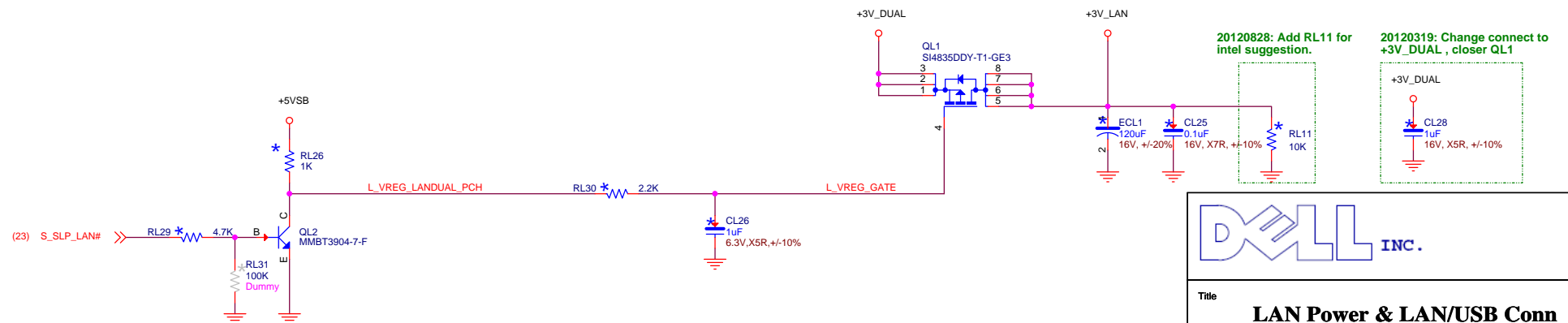
# LAN CONNECTOR

20120214: NIC\_USB need apply HH P/N into CIS  
 20120217: NIC\_USB Change to JFM38U1B-21M5-4F , need apply HH P/N into CIS  
 20120229: NIC\_USB Change to JFM38U1B-21M5-4F, link from M disk



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# LAN POWER



Title		
LAN Power & LAN/USB Conn		
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•



•



## A










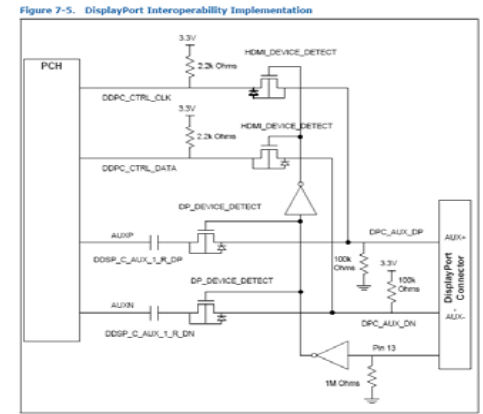
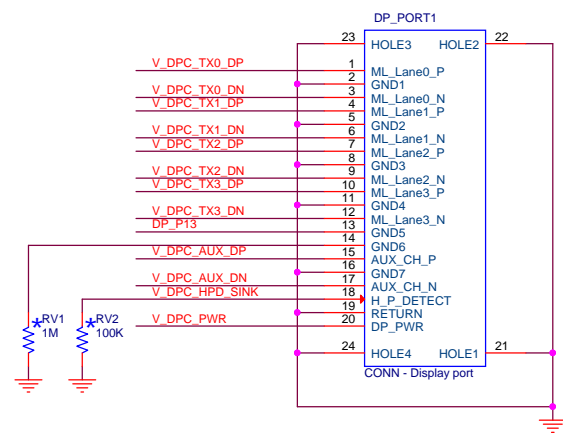
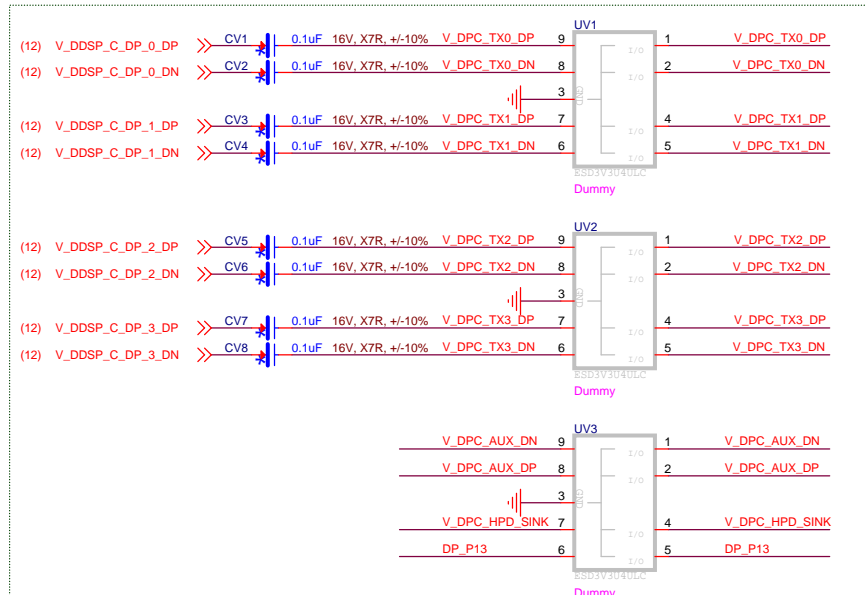
www.aitech1.ru

	
Title <b>TBD</b>	
DWG NO <b>Amazon SFF</b>	Rev <b>A00</b>
Date: Tuesday, March 12, 2013 Sheet 37 of 66	

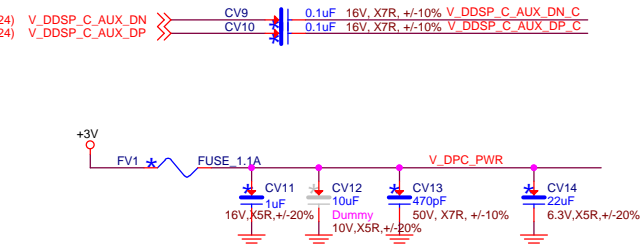
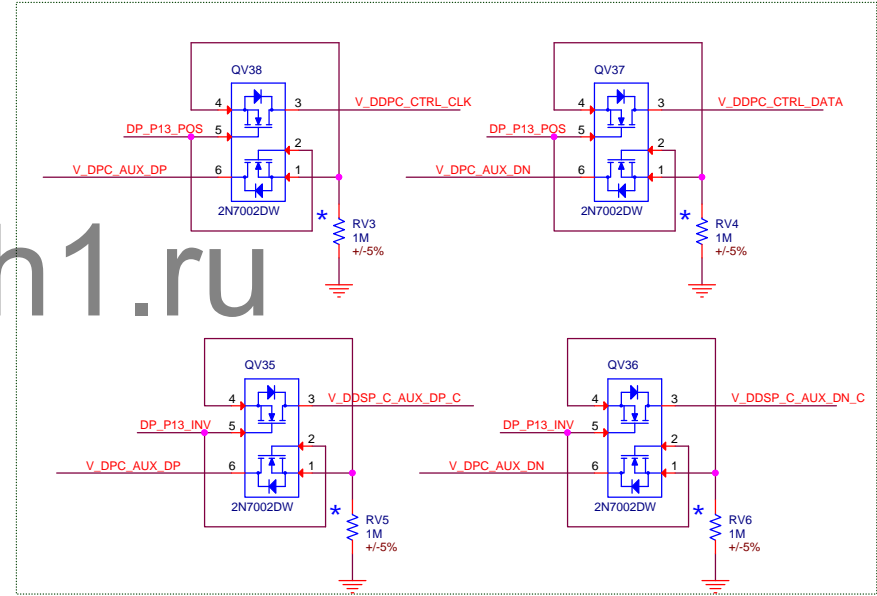
www.aitech1.ru

		
Title <b>TBD</b>		
DWG NO	<b>Amazon SFF</b>	Rev <b>A00</b>
Date: Tuesday, March 12, 2013	Sheet 38 of 66	1

20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON\_ESD3V3U4ULC

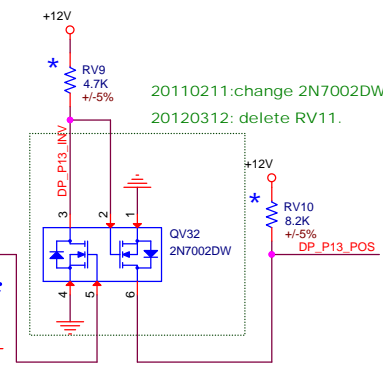
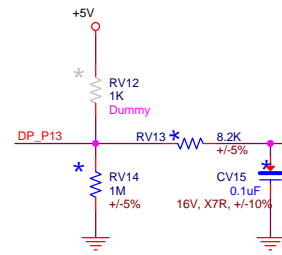
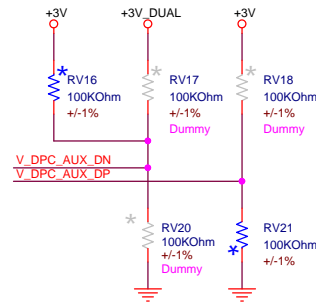
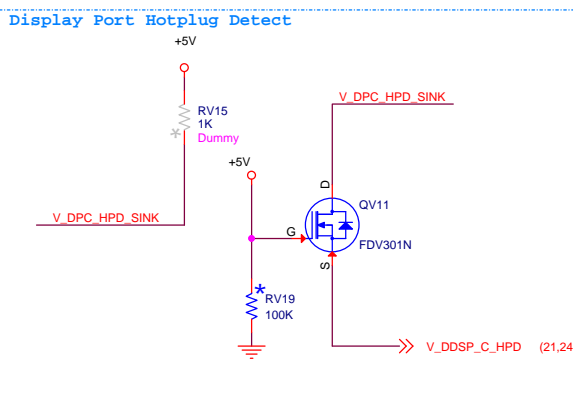


20110211:change 2N7002DW for cost down.




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(24) V\_DDPC\_CTRL\_CLK << V\_DDPC\_CTRL\_CLK  
(24) V\_DDPC\_CTRL\_DATA << V\_DDPC\_CTRL\_DATA



20110211:change 2N7002DW for cost down.  
20120312: delete RV11.



**Display Port 1**

DWG NO **Amazon SFF** Rev **A00**

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20120521: Delete UV8 ; UV7, UV9, UV10 change to INFINEON\_ESD3V3U4ULC

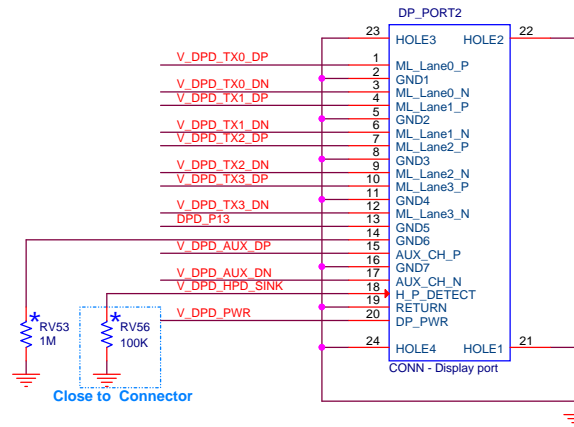
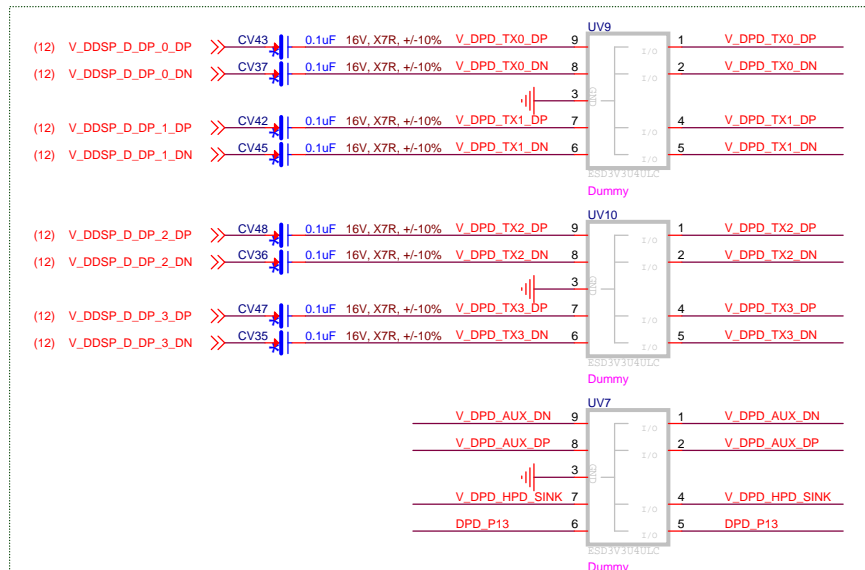
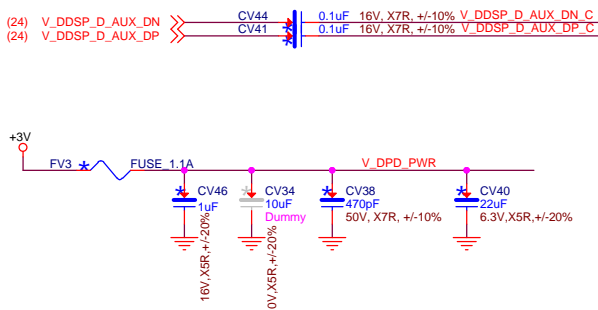
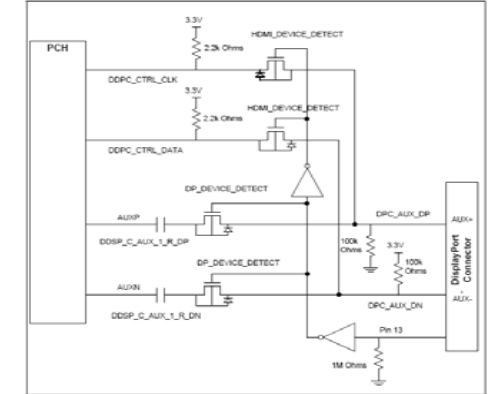


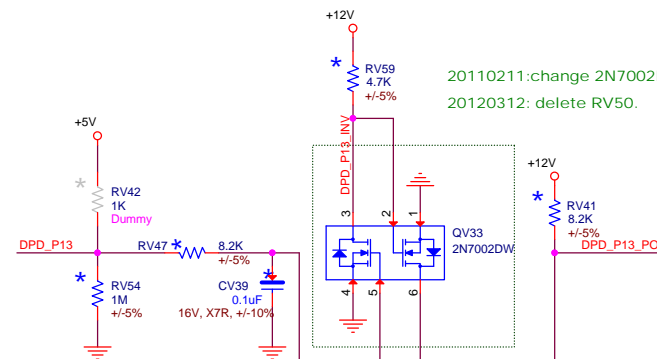
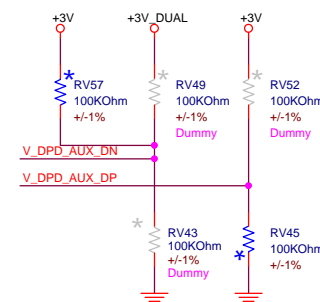
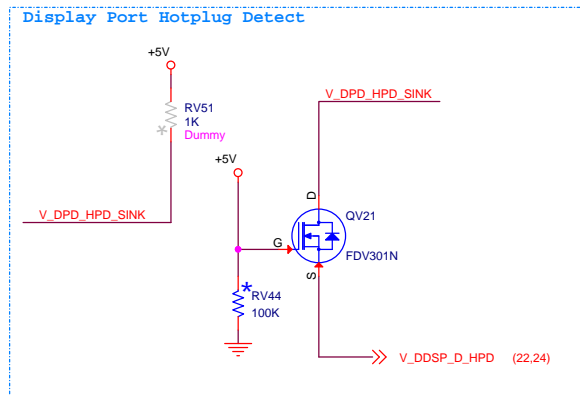
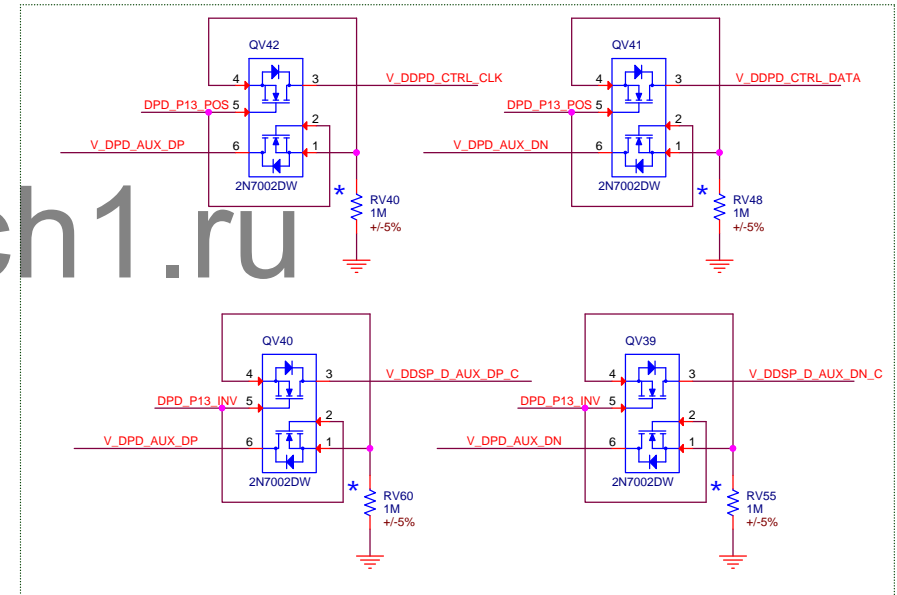
Figure 7-5. DisplayPort Interoperability Implementation



(24) V\_DDPD\_CTRL\_CLK << V\_DDPD\_CTRL\_CLK

(24) V\_DDPD\_CTRL\_DATA << V\_DDPD\_CTRL\_DATA

20110211:change 2N7002DW for cost down.

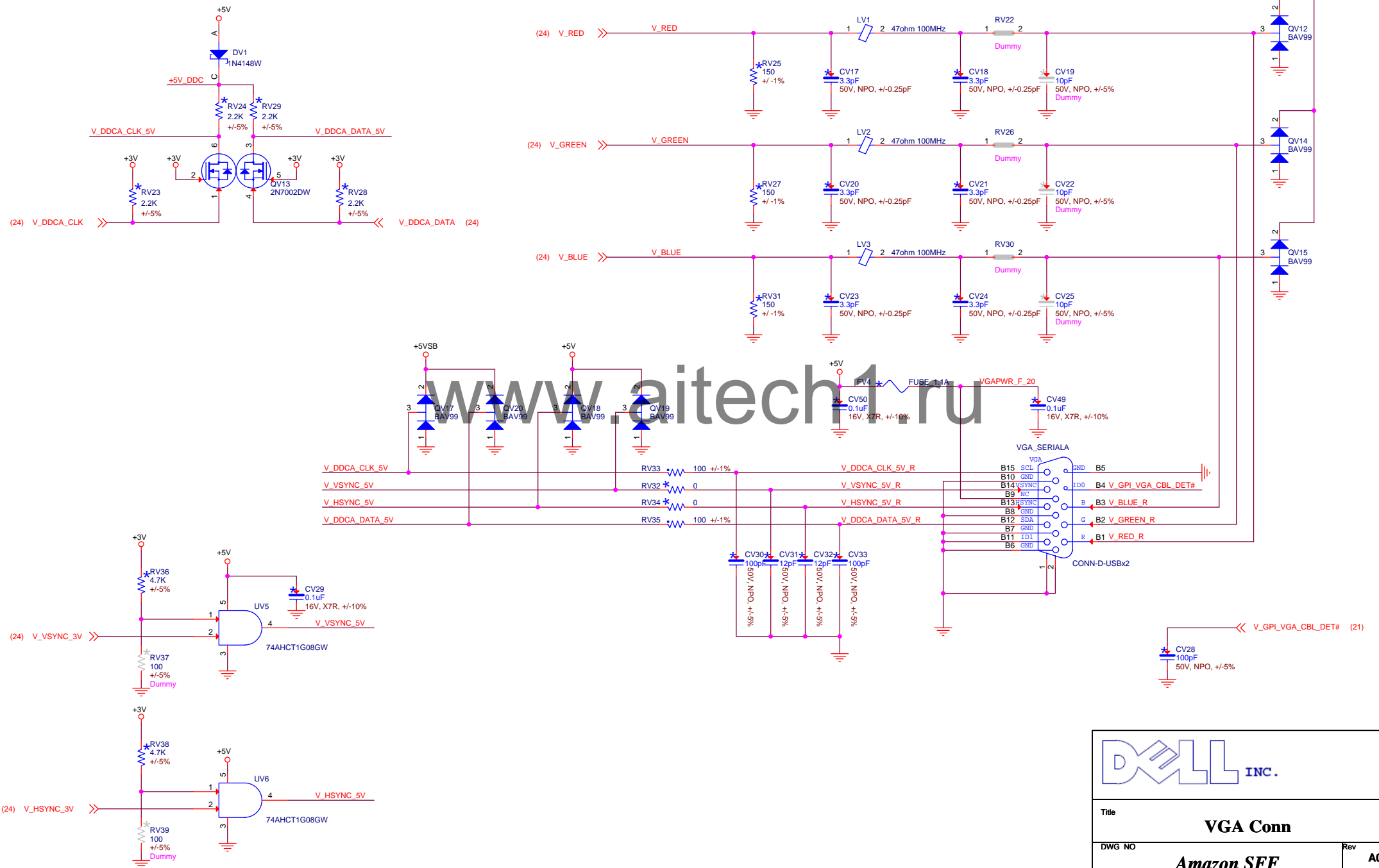


20110211:change 2N7002DW for cost down.

20120312: delete RV50.

<b>Display Port 2</b>		
Title DWG NO Date: Tuesday, March 12, 2013	Amazon SFF	Rev A00 Sheet 40 of 66

## VGA Connector

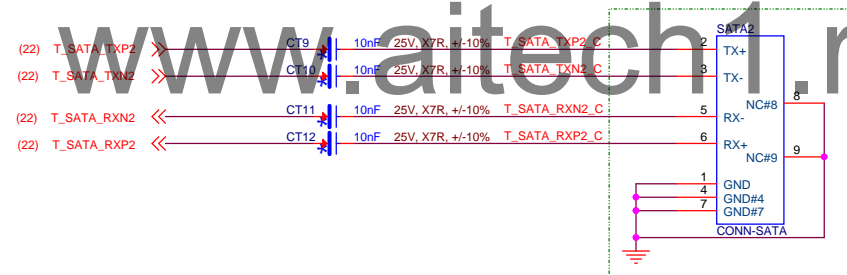
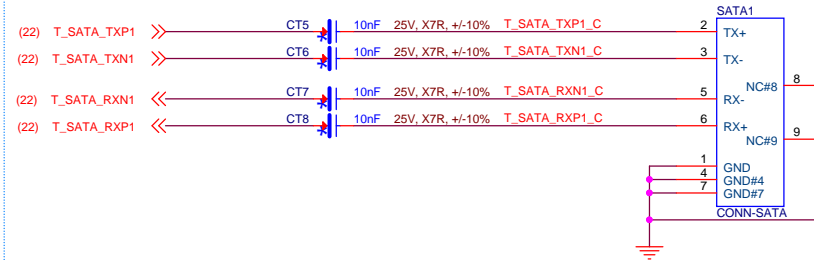
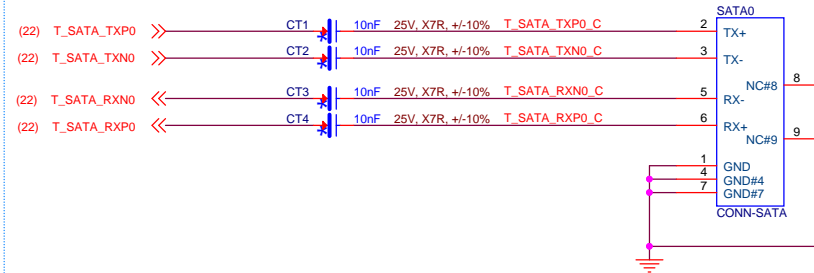


Title	<b>VGA Conn</b>
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DWG NO	Rev
<i>Amazon SFF</i>	A00

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# SATA Gen.3



20120312: SATA2 change to SATA2.0 connector



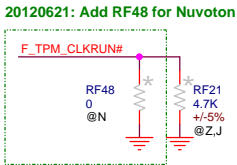
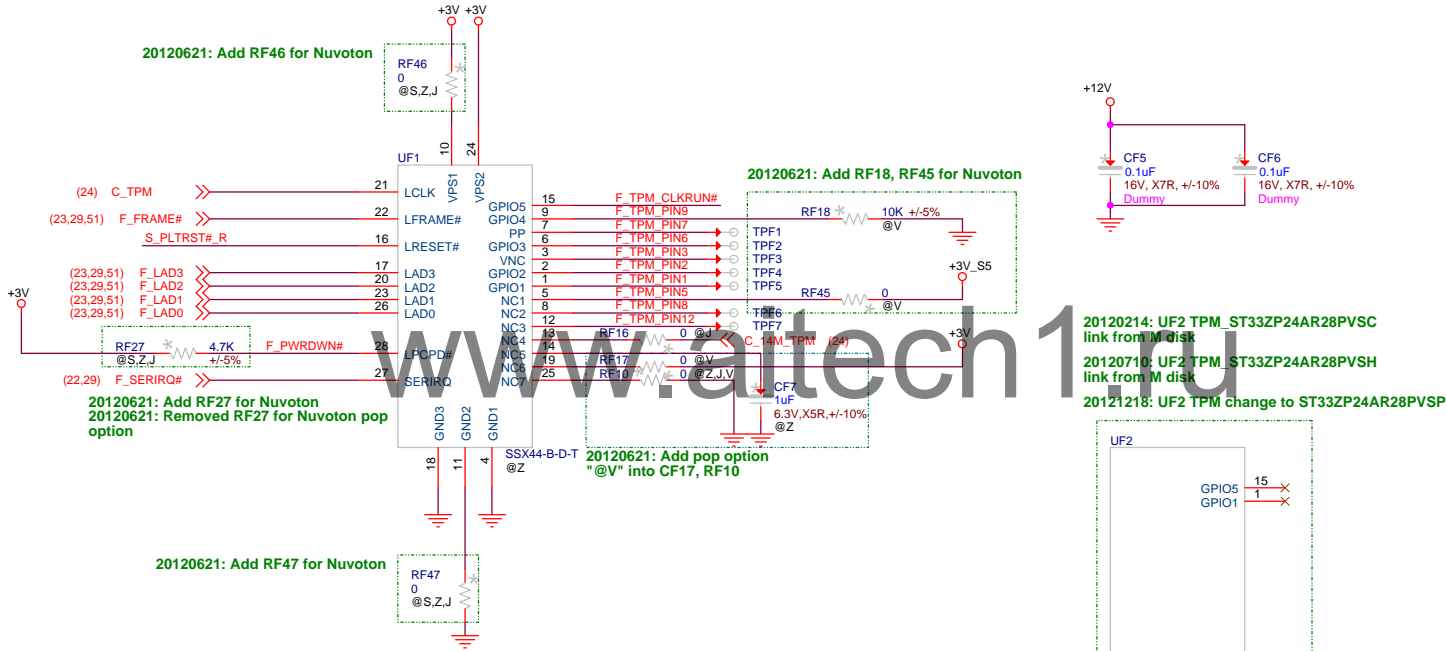
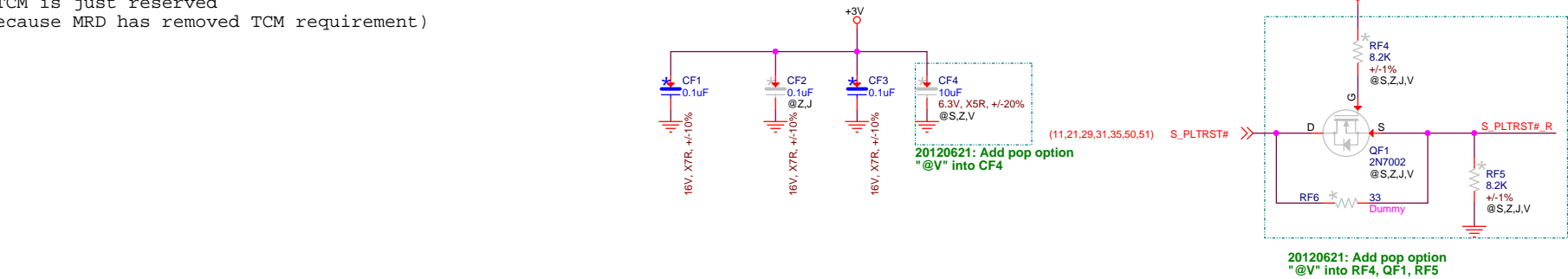
Title		
SATA Conn		
DWG NO	Amazon SFF	Rev A00
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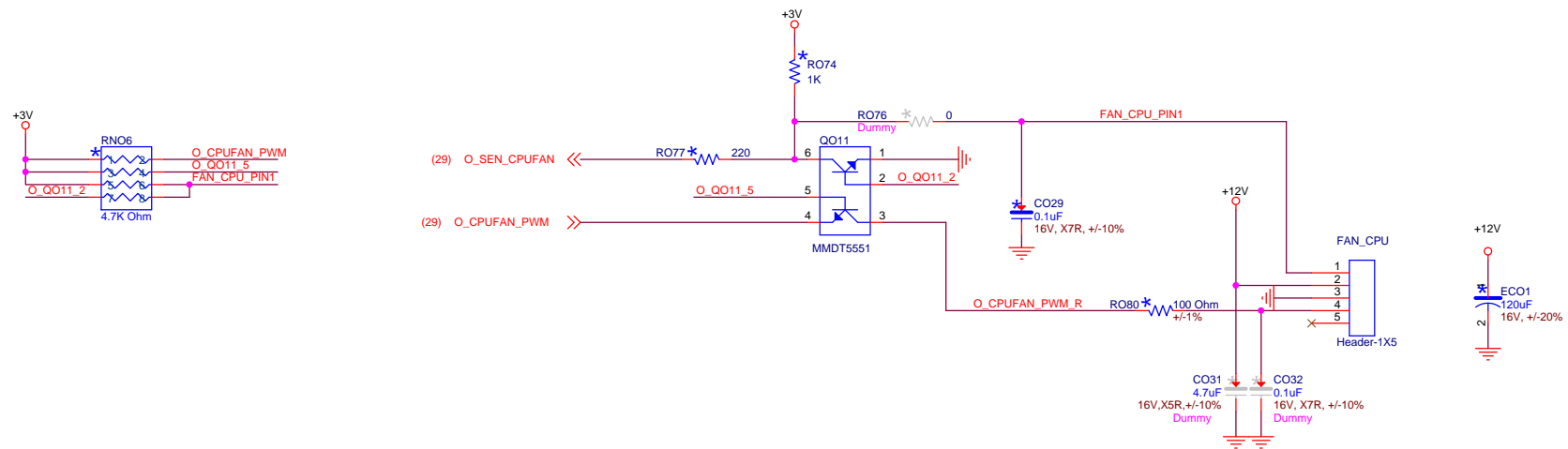


TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

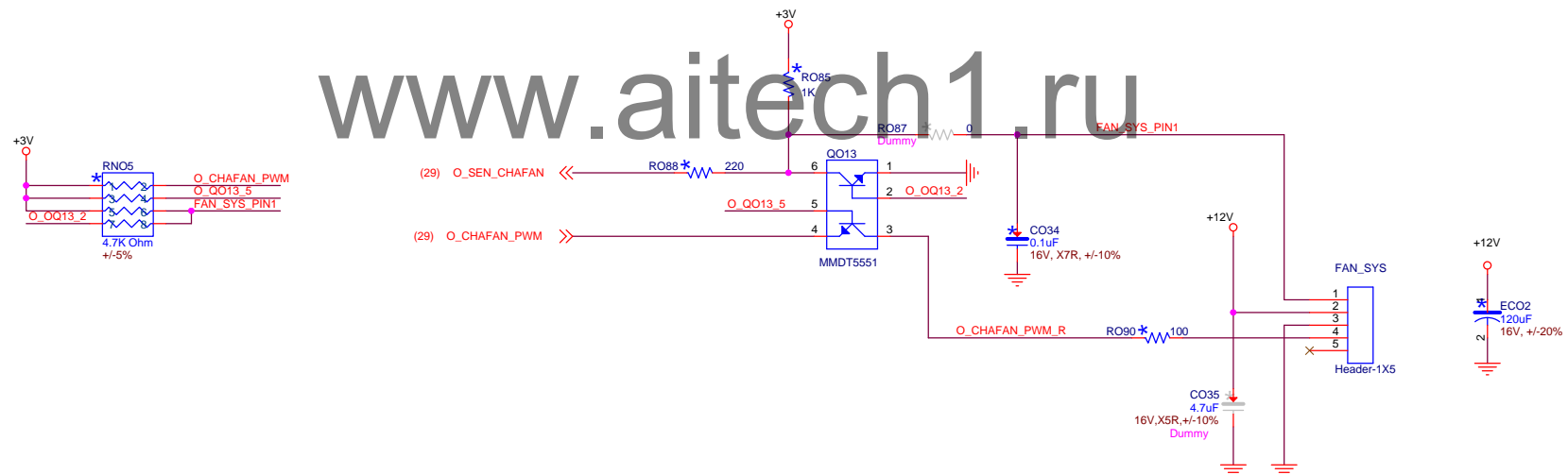
(Default) ST Micro	POP S
ZTE	POP Z
Jetway	POP J
Nuvoton	POP V



## CPU Fan



**SYS Fan**



**PSU Fan**



	Title
--	-------

**FAN**

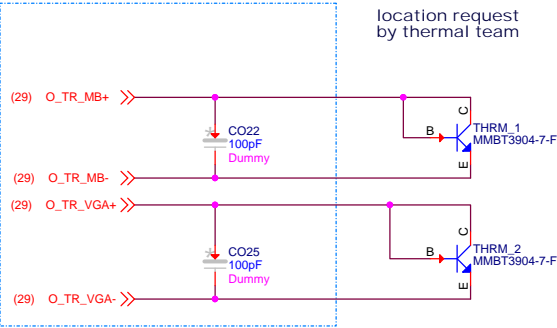
DWG NO
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### Amazon SFF

Rev	<b>A00</b>
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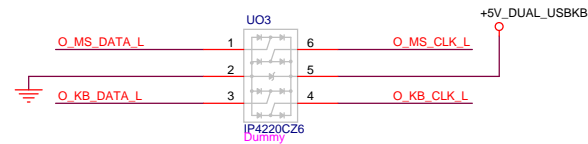
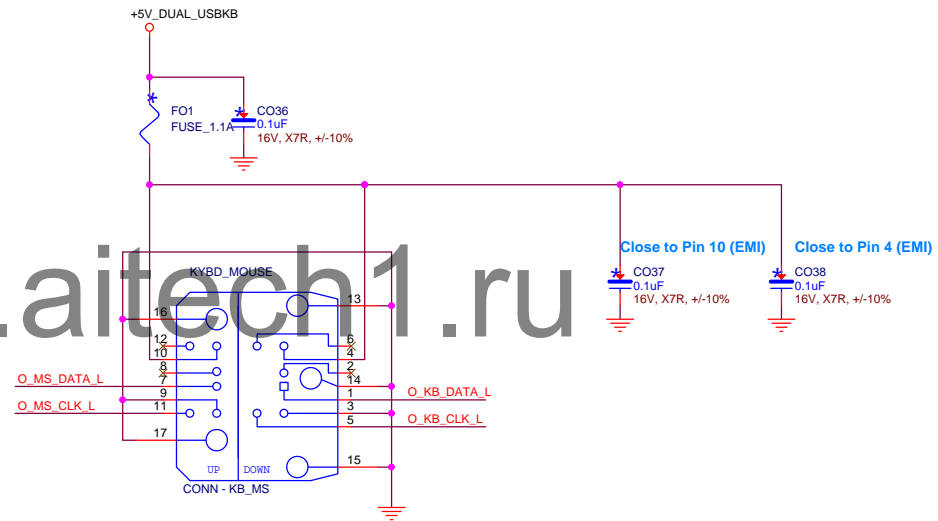
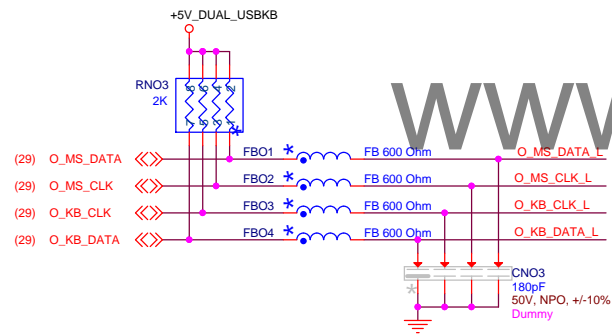


Title  
**Thermal Sensor**

DWG NO  
**Amazon SFF**

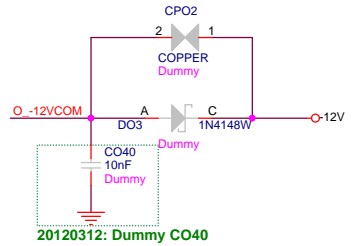
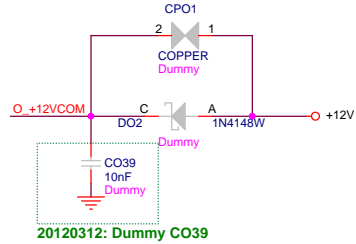
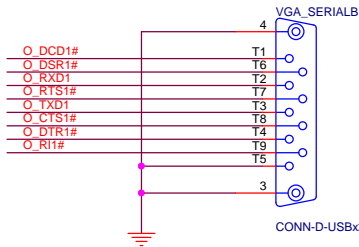
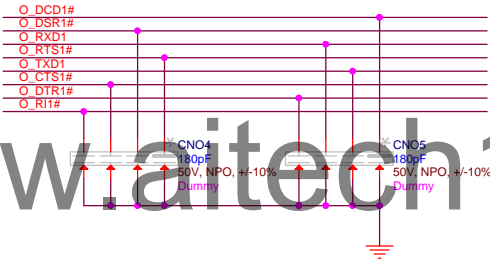
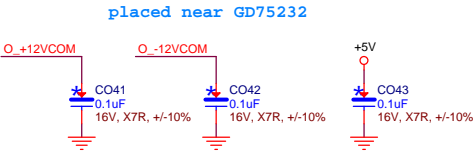
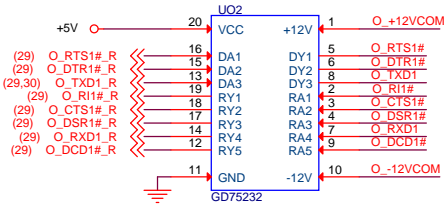
Rev  
**A00**

KB/MS



Title			PS2 Conn		
DWG NO			Rev		
Amazon SFF			A00		
Date:	Tuesday, March 12, 2013	Sheet	47	of	66

Serial Port 1



**INC.**

Title

**COM1**

DWG NO

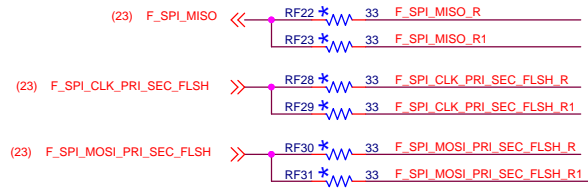
**Amazon SFF**

Rev

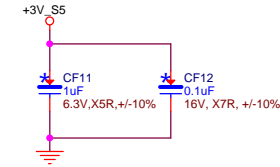
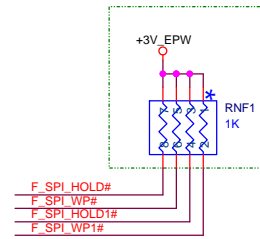
**A00**

Date: Tuesday, March 12, 2013

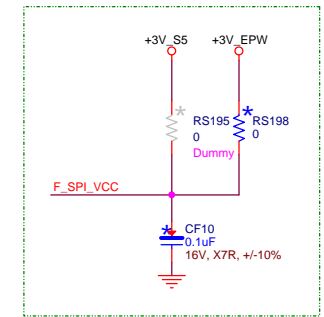
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20120515: RNF1 pull-up  
change to +3V\_EPW



20120515: Add RS195, RS198 for SPI ROM option.  
20120618: Stuffed RS198, Dummy RS195



## SPI\_4MB

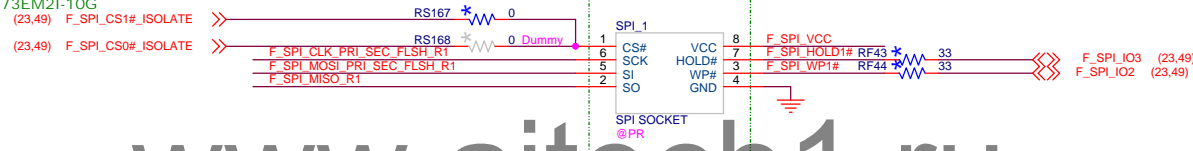
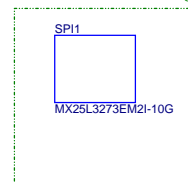
20110530: SPI1 Change to 4M

20120216: SPI1 Change to WINBOND\_W25Q32BVSSIG

20120301: SPI1 link from Dell CIS

20121221: SPI1 change to W25Q32FVSSIQ

20121225: SPI1 change to MXIC\_MX25L3273EM2I-10G



20120216: SPI\_1 add BOM option

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## SPI\_8MB

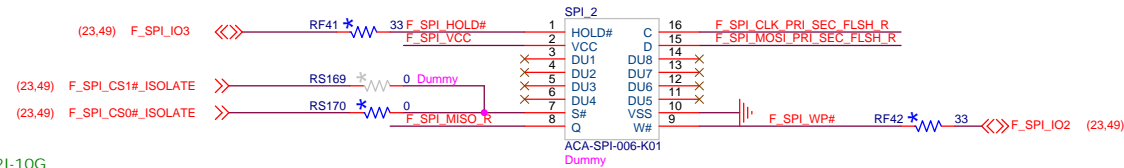
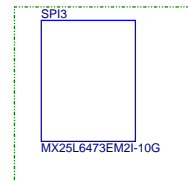
20120216: SPI2 rename to SPI3 and Change to 8M , 8 pins flash

20120216: SPI3 and Change to 8M , 8 pins flash, WINBOND\_W25Q64FVSSIG

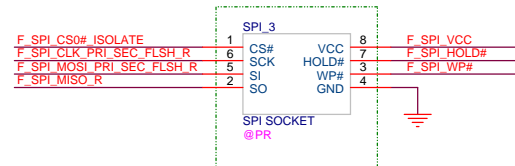
20120301: SPI3 link from Dell CIS

20121221: SPI3 change to W25Q64FVSSIQ

20121225: SPI3 change to MXIC\_MX25L6473EM2I-10G

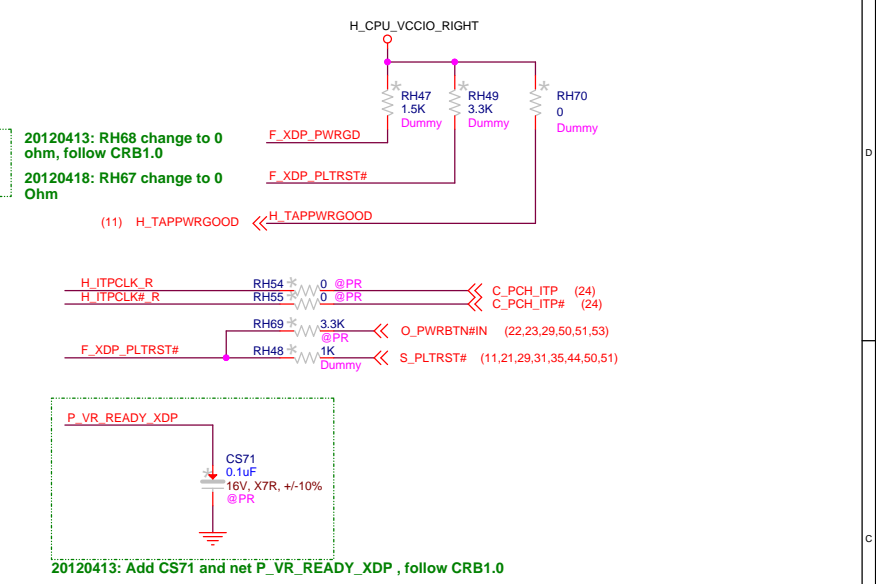
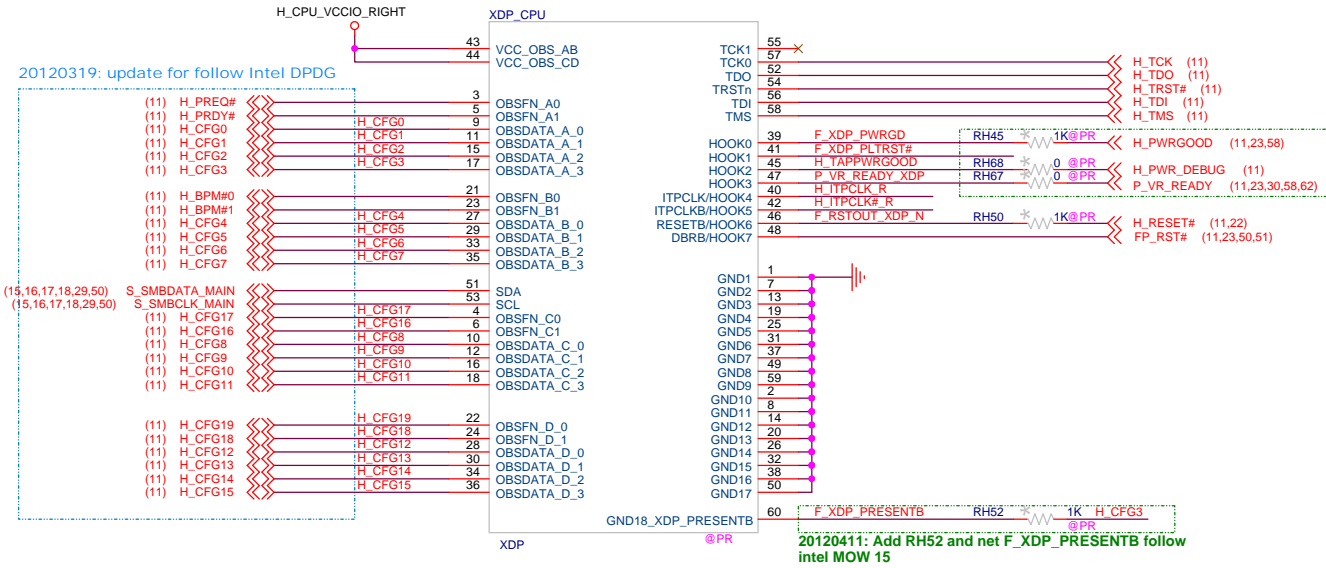


20120216: SPI\_3 add BOM option

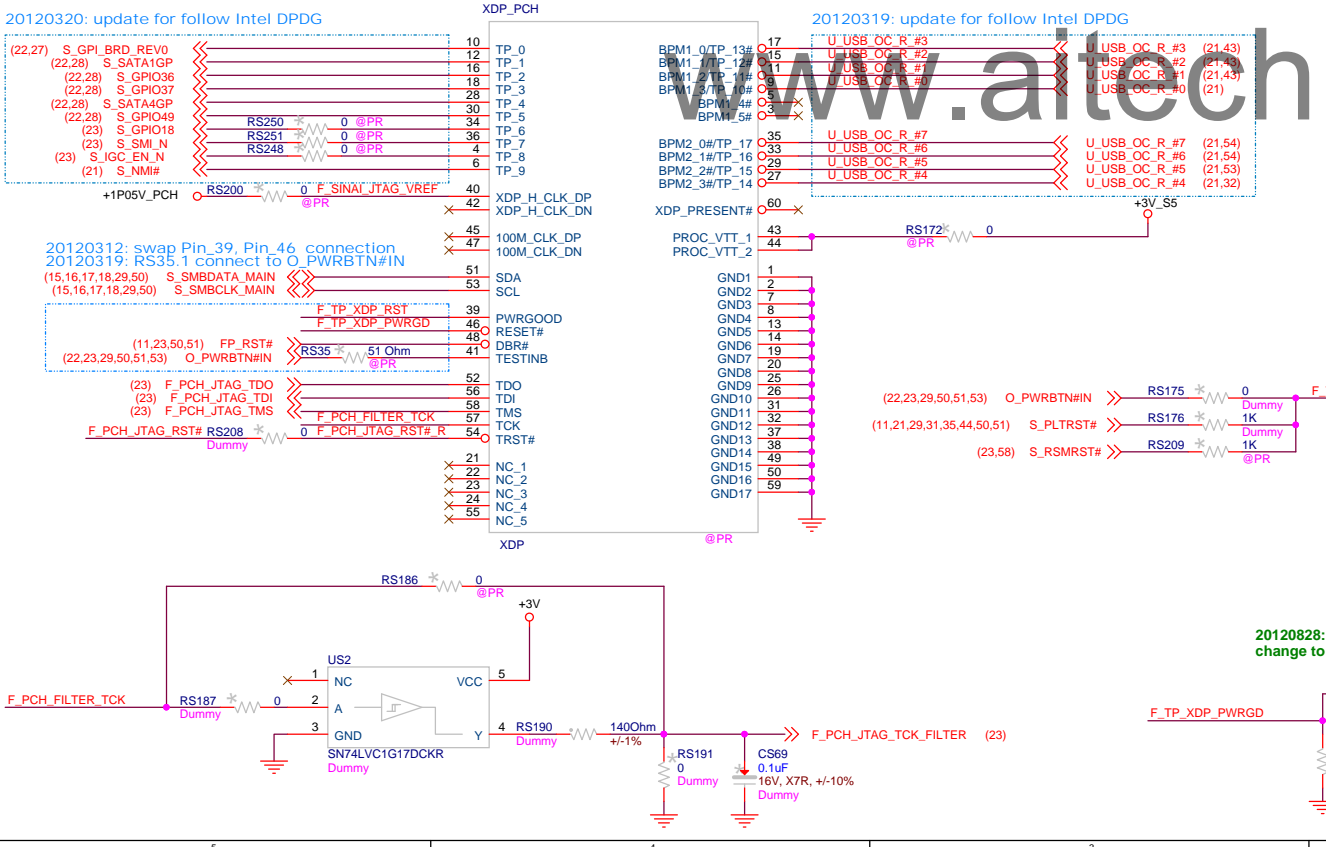


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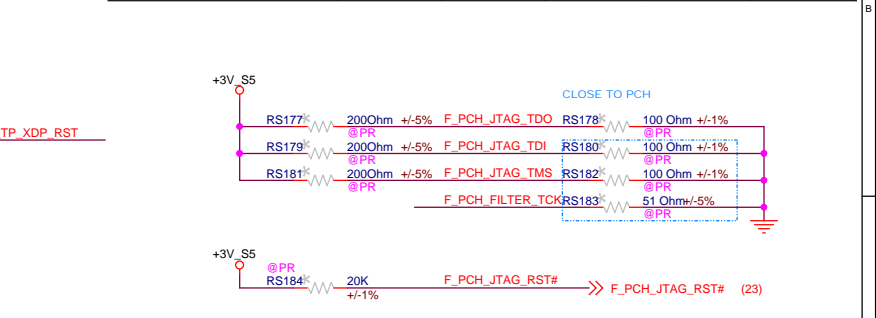
XDP Connector - CPU



XDP Connector - PCH



2009/12/21 Update JTAG Table	PCH JTAG Enable		PCH JTAG Disable	
	ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms <sup>1</sup>	No Stuff
	RS178	No Stff	100 Ohms <sup>1</sup>	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms
	RS182	100 Ohms	100 Ohms	10K Ohms
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff



Title

**XDP**

DWG NO

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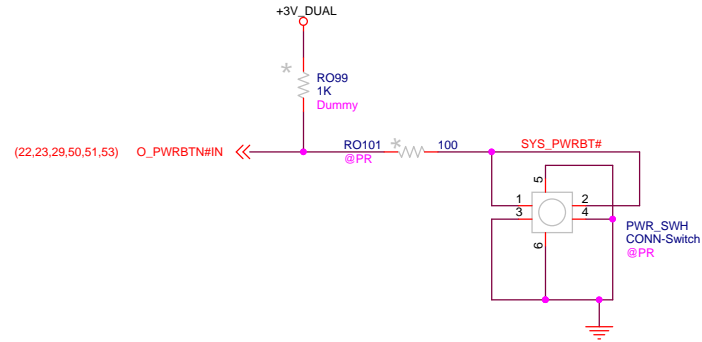
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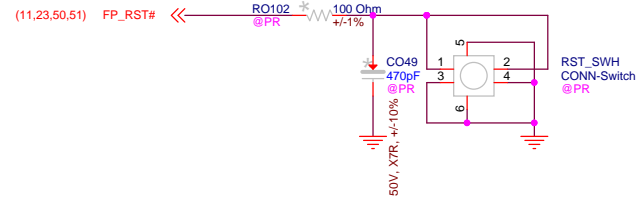
**A00**



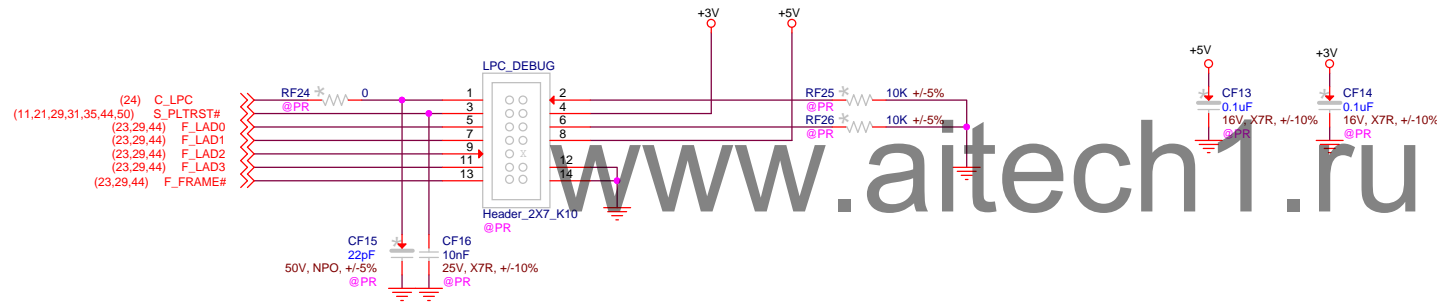
## Power Bottom



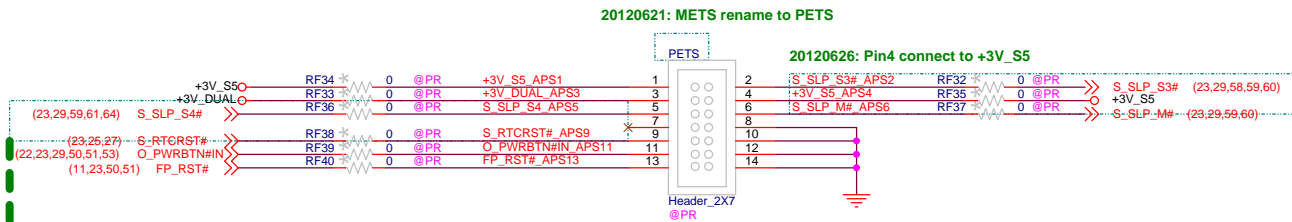
## Reset Bottom



## LPC DEBUG



## APS Debug



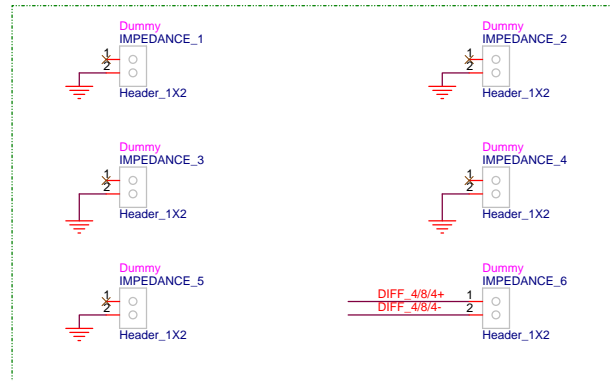
20120626: Pin7 net rename to +3V\_DUAL\_APS7 and add RF49 connect to +3V\_DUAL  
20120626: Pin7 let NC

Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

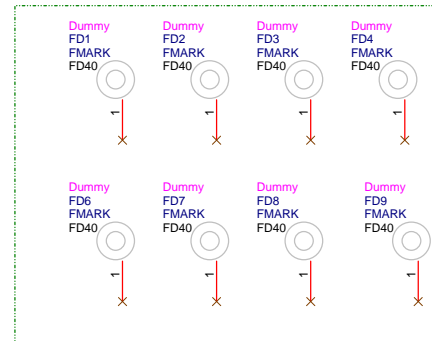


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Pilot Run Conn		
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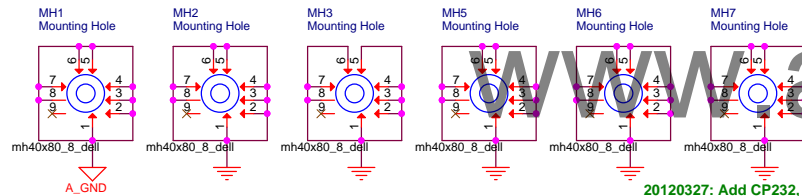
20120312: IMPEDANCE\_2, IMPEDANCE\_5 Pin#1 left NC



20120319: Delete FD10, FD11



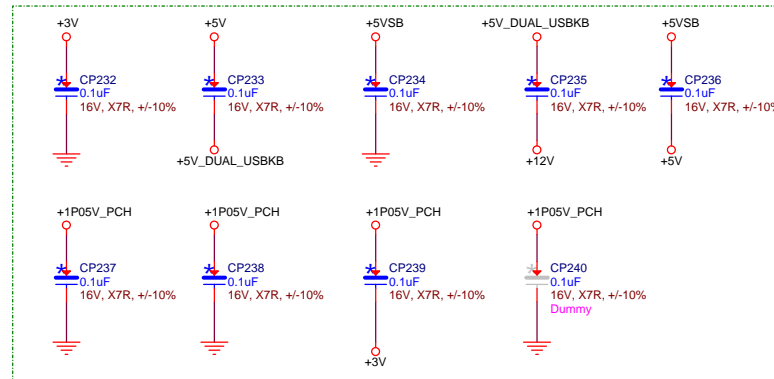
20120307: delete MH4



20120315: Delete CP239, CP240, CP241



20120327: Add CP232, CP233  
20120628: CP232 change connection to +3V and GND  
20120629: Add CP234 connection to +5VSB and GND  
20120906: Add CP235, CP236 for DFE request.  
20121217: Add CP237, CP238 for across moat.  
20121218: Add CP239 for across moat. Add CP240 for power noise

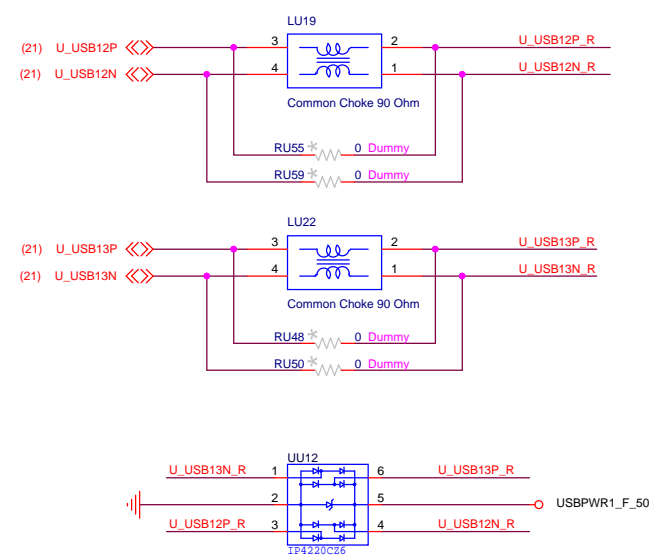
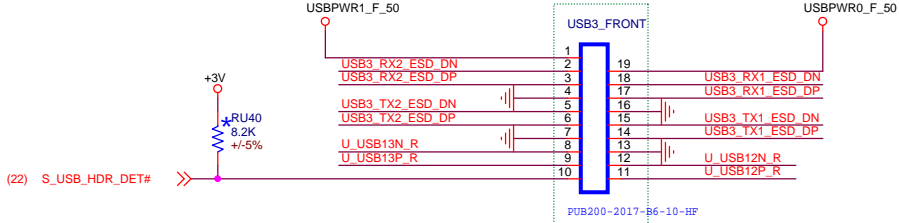
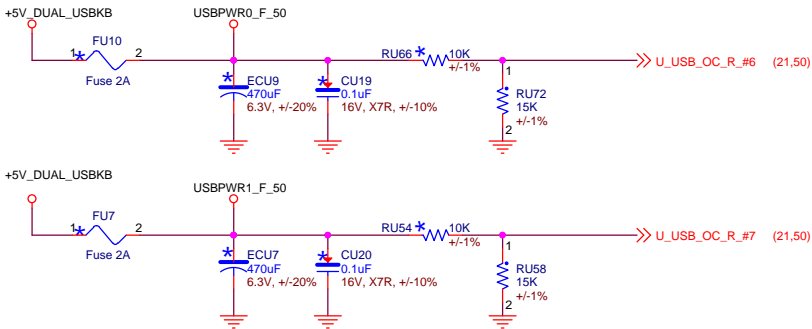


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EMI	
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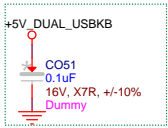


Front USB/LED Header

20120214: USB3\_FRONT connector change to PUB200-2017-B5-10-HF.  
20121225: USB3\_FRONT connector change to PUB200-2017-B6-10-HF.



20120312: Dummy CO51



20120315: Dummy LU20, LU21, LU18, LU17 : Stuffed RU53, RU49, RU57, RU60, RU46, RU56, RU45, RU47  
20120320: CO81, CO78, CO80, RU53, RU49, RU57, RU60, RU46, RU56, RU45, RU47, UU10, UU11

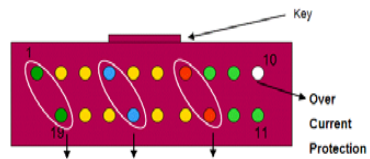
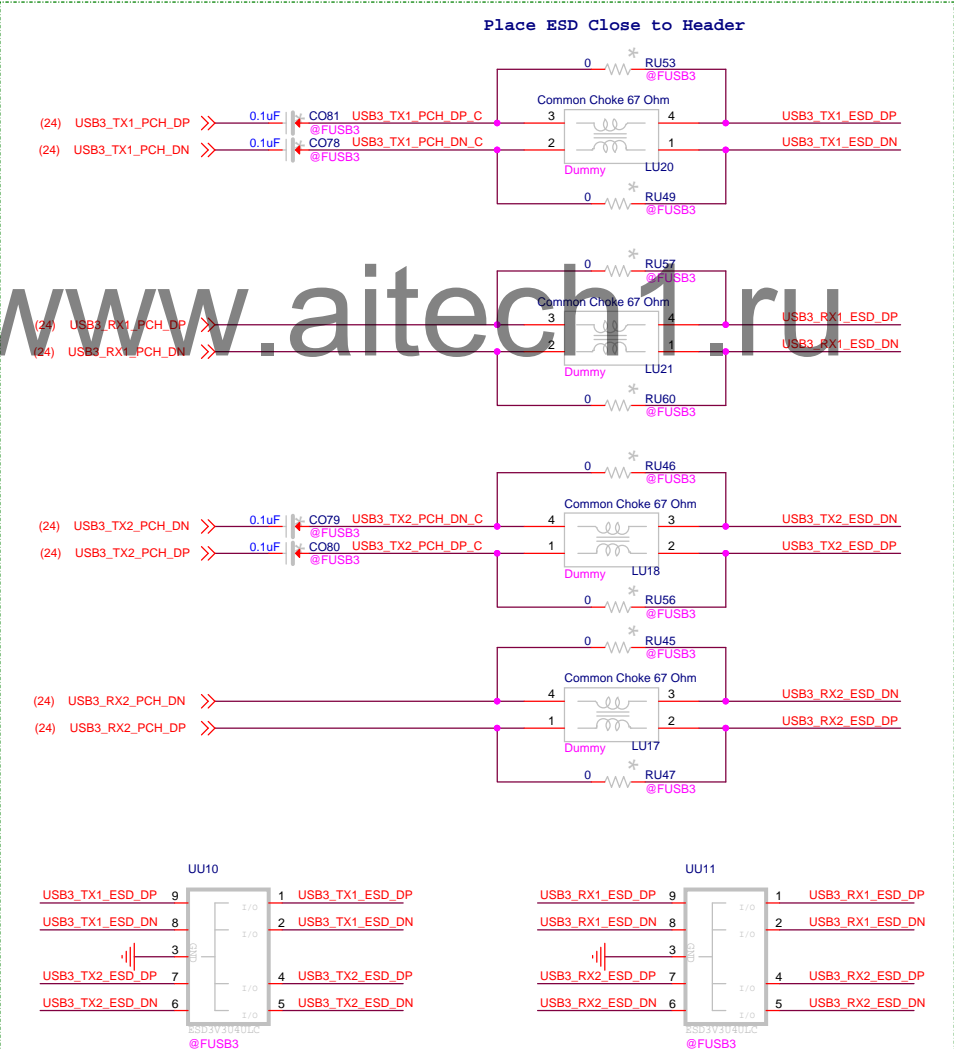
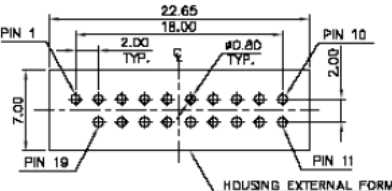
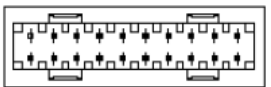
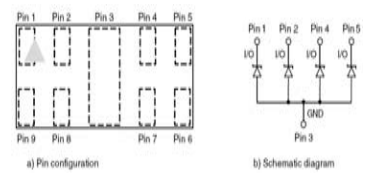


Figure 2-1: USB3 ICC pin numbering



RECOMMENDED P.C.B. LAYOUT  
TOLERANCE IS ±0.05



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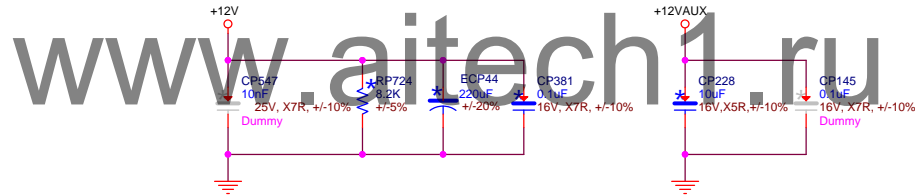
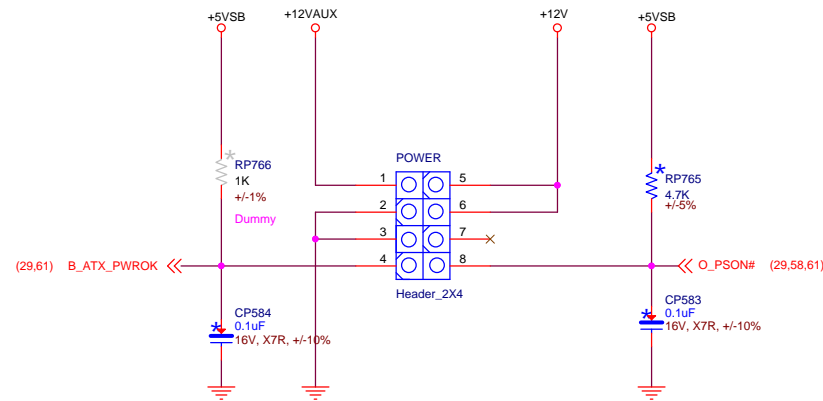
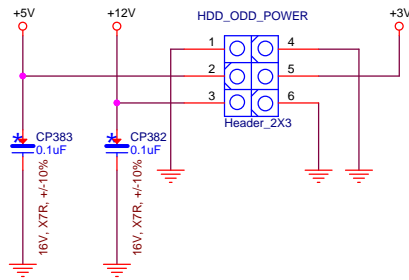
	
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# ATX POWER CONNECTOR

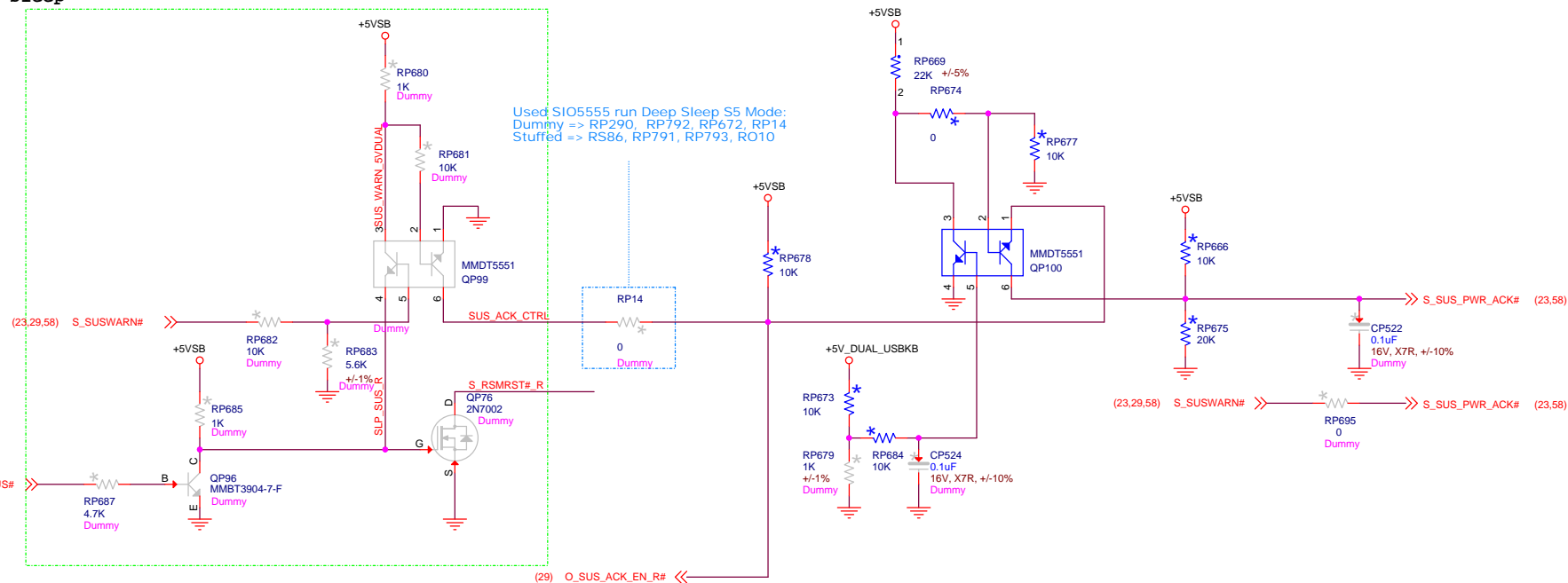
For ODD and HDD



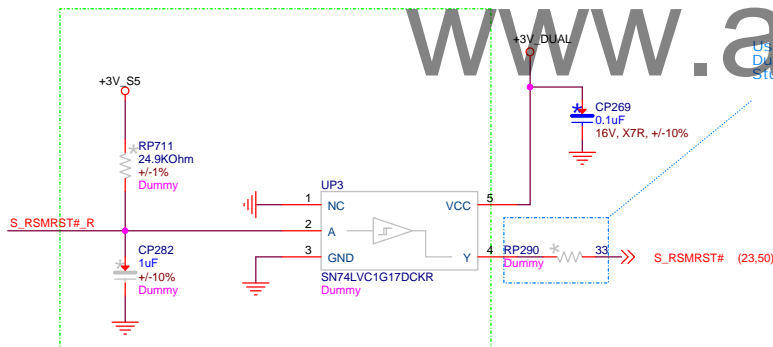
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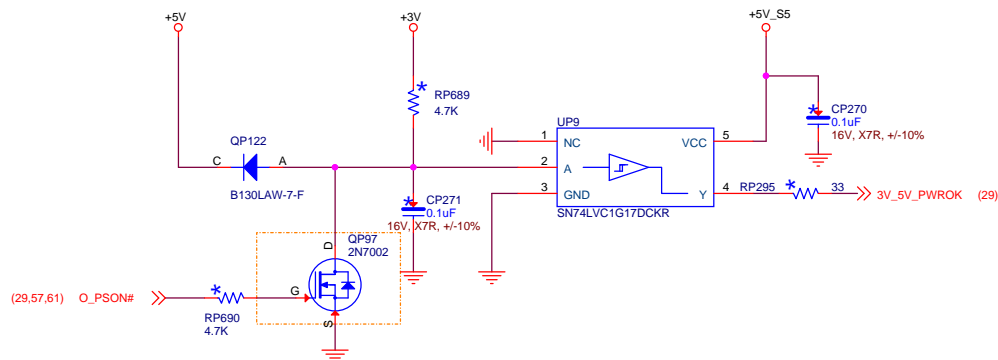
# For Deep Sleep



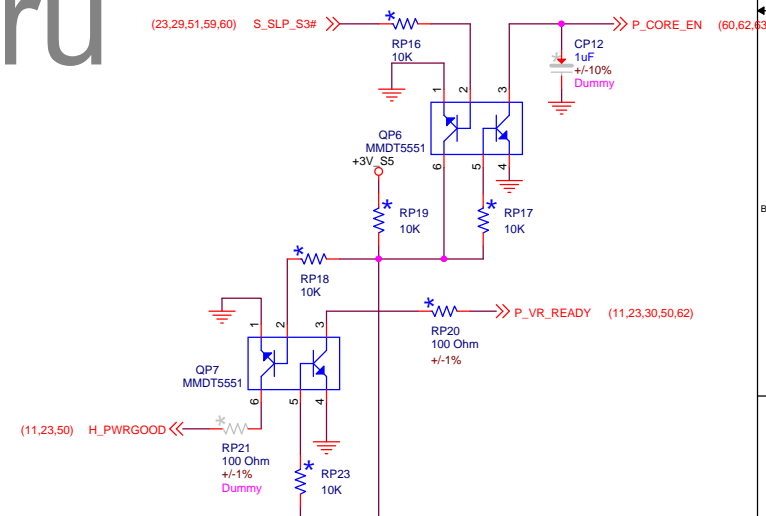
# RESUME RESET Logic



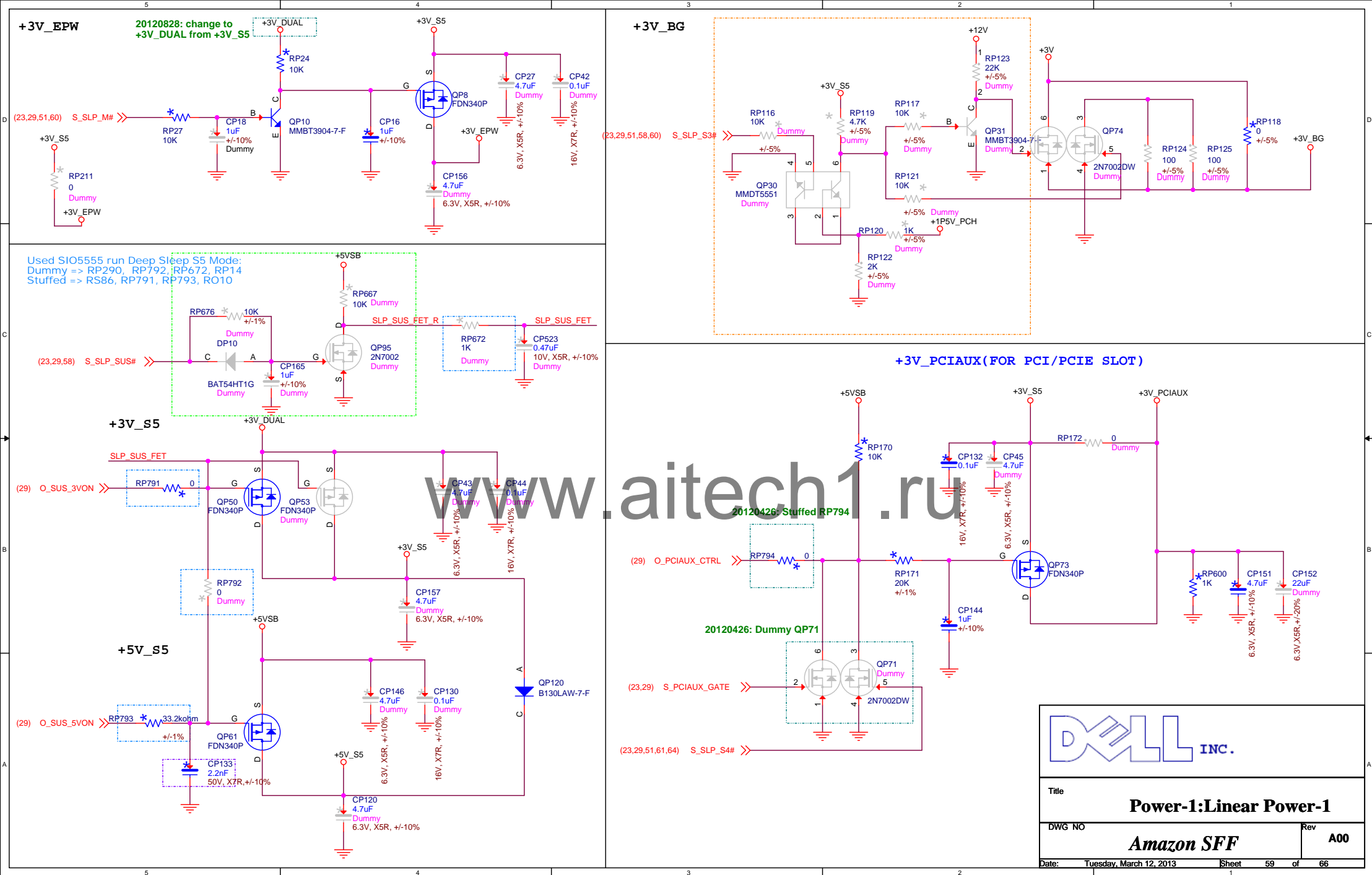
# New ATXPWROK



# VR\_READY DEFENSIVE



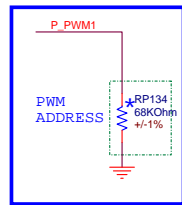
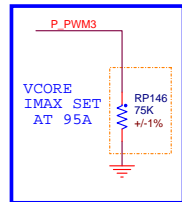
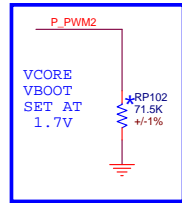
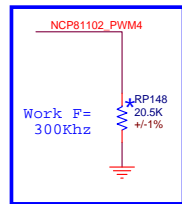
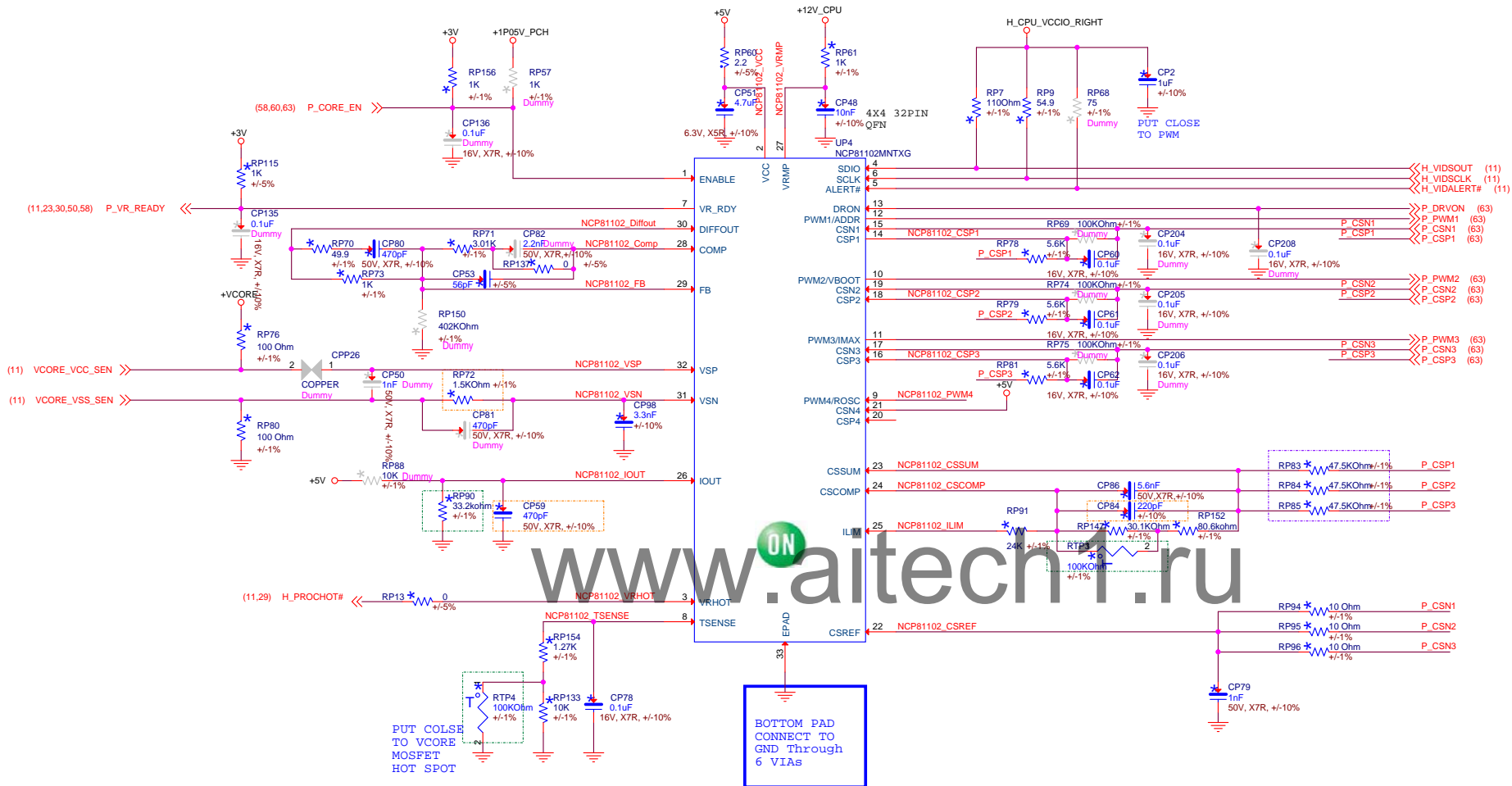
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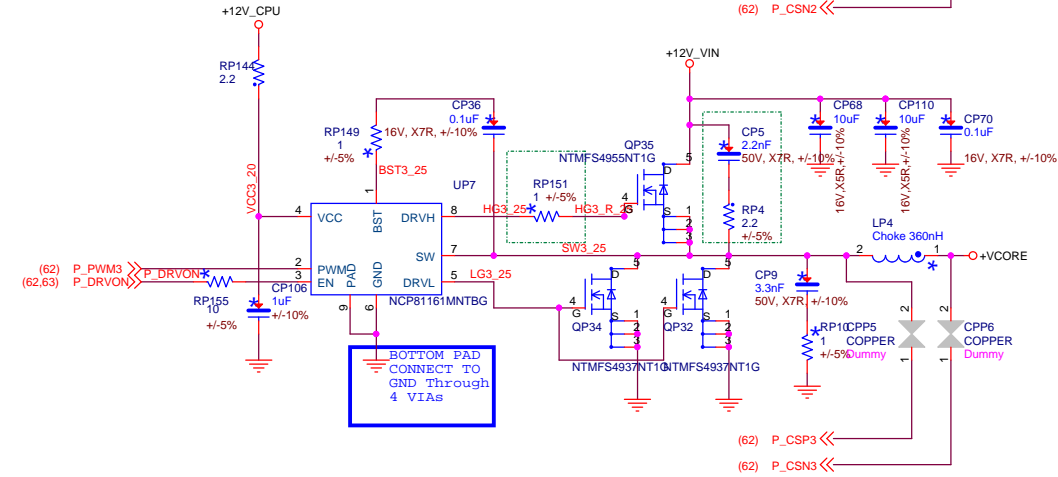
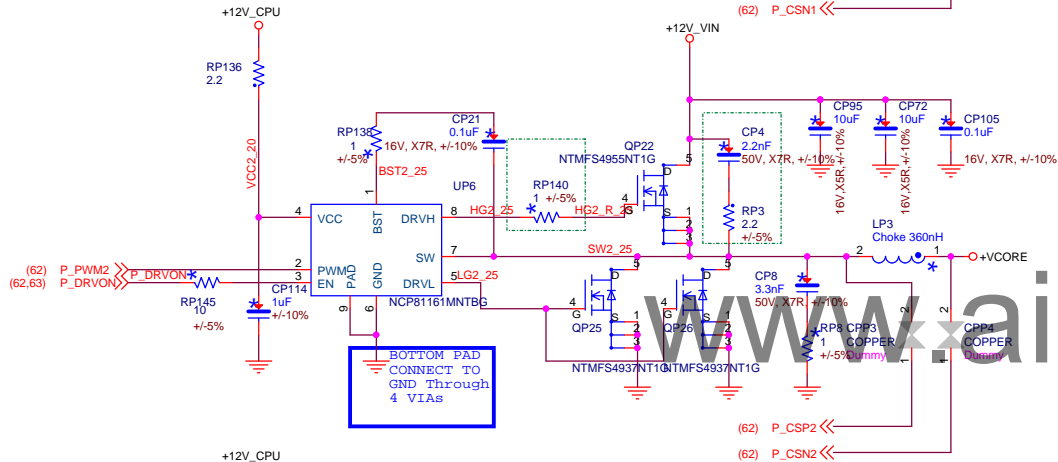
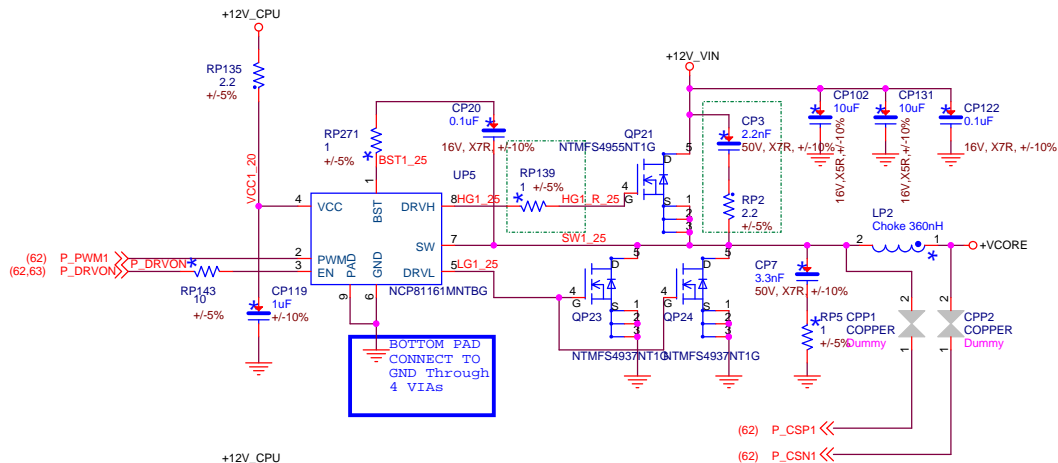
# SharkBay VR12.5 POWER CKT -3PHASE



Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250Kh	30.9K	340khz	61.9K	430Khz	105K	520 Khz	165K	610Khz
12K	260Kh	34K	350khz	64.9K	440Khz	110K	530Khz	174K	620Khz
14K	270Kh	36.5K	360khz	69.8K	450Khz	115K	540Khz	182K	630Khz
16.2K	280Kh	40.2K	370khz	73.2K	460Khz	121K	550Khz	191K	640Khz
18.2K	290Kh	43.2K	380khz	78.7K	470Khz	130K	560Khz	200K	650Khz
20.5K	300Kh	46.4K	390khz	82.5K	480Khz	137K	570Khz		
23.2K	310Kh	49.9K	400khz	88.7K	490Khz	143K	580Khz		
25.5K	320Kh	53.6K	410khz	93.1K	500Khz	150 K	590Khz		
28K	330Kh	57.6K	420khz	100K	510Khz	158 K	600Khz		

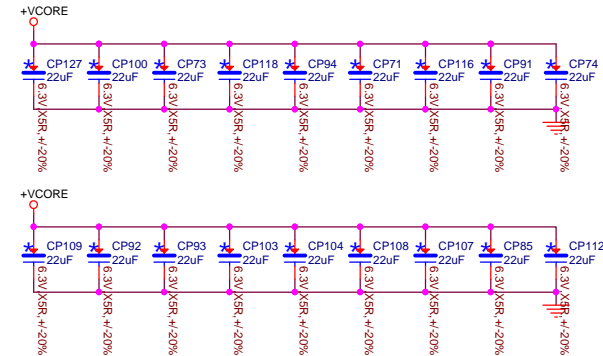


Title			
<b>Power-4:VCore</b>			
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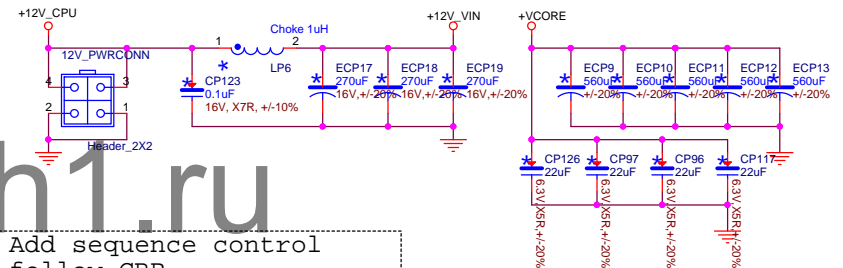
# CAD NOTE:

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

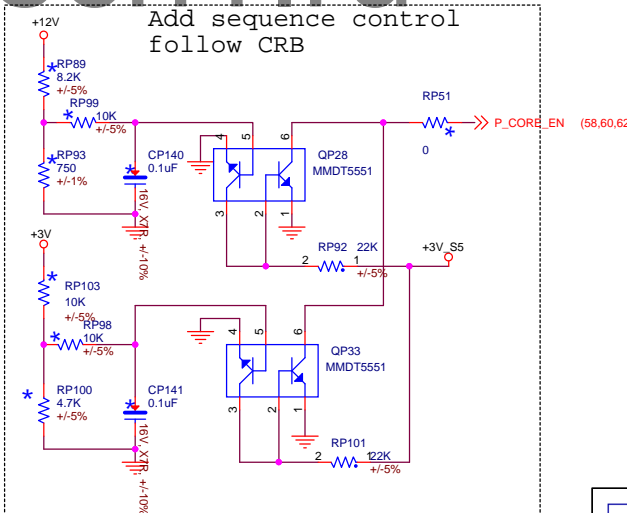


# CAD NOTE:

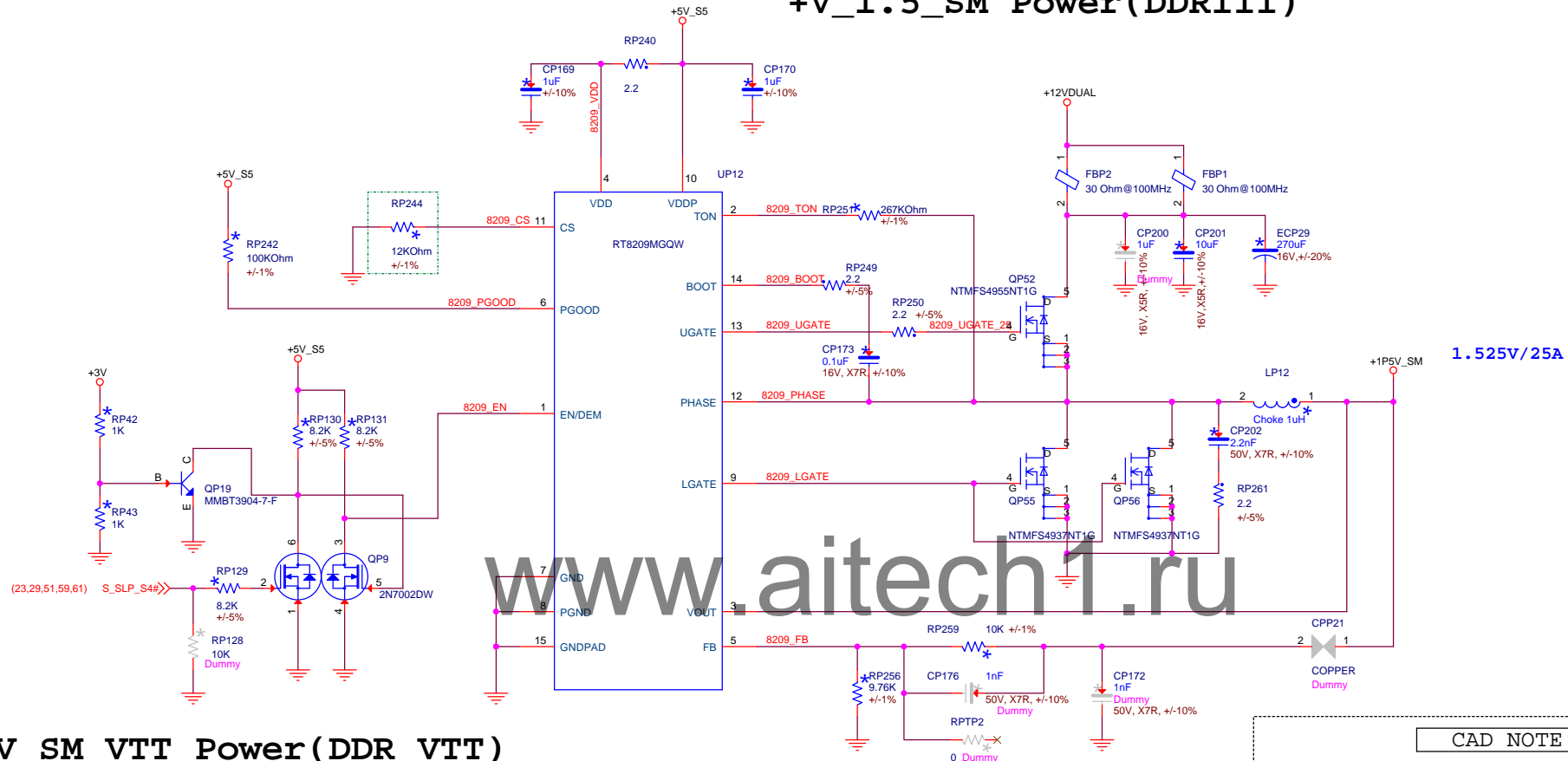
PLACE CAPS AT TOP SOCKET EDGE



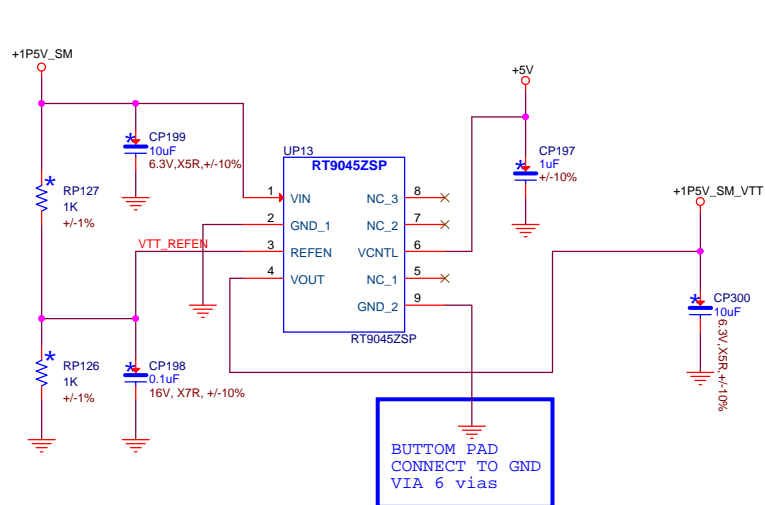
Add sequence control follow CRB



## +V\_1.5\_SM Power(DDRIII)

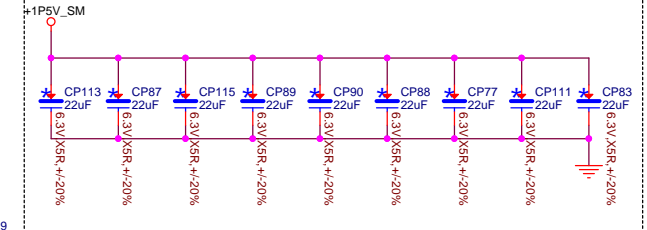


## +V\_SM\_VTT Power(DDR VTT)



### CAD NOTE:

PLACE ALL 0805 CAPS INSIDE  
CPU SOCKET CAVITY



Title  
**Power-6: DDR3**

DWG NO  
**Amazon SFF**

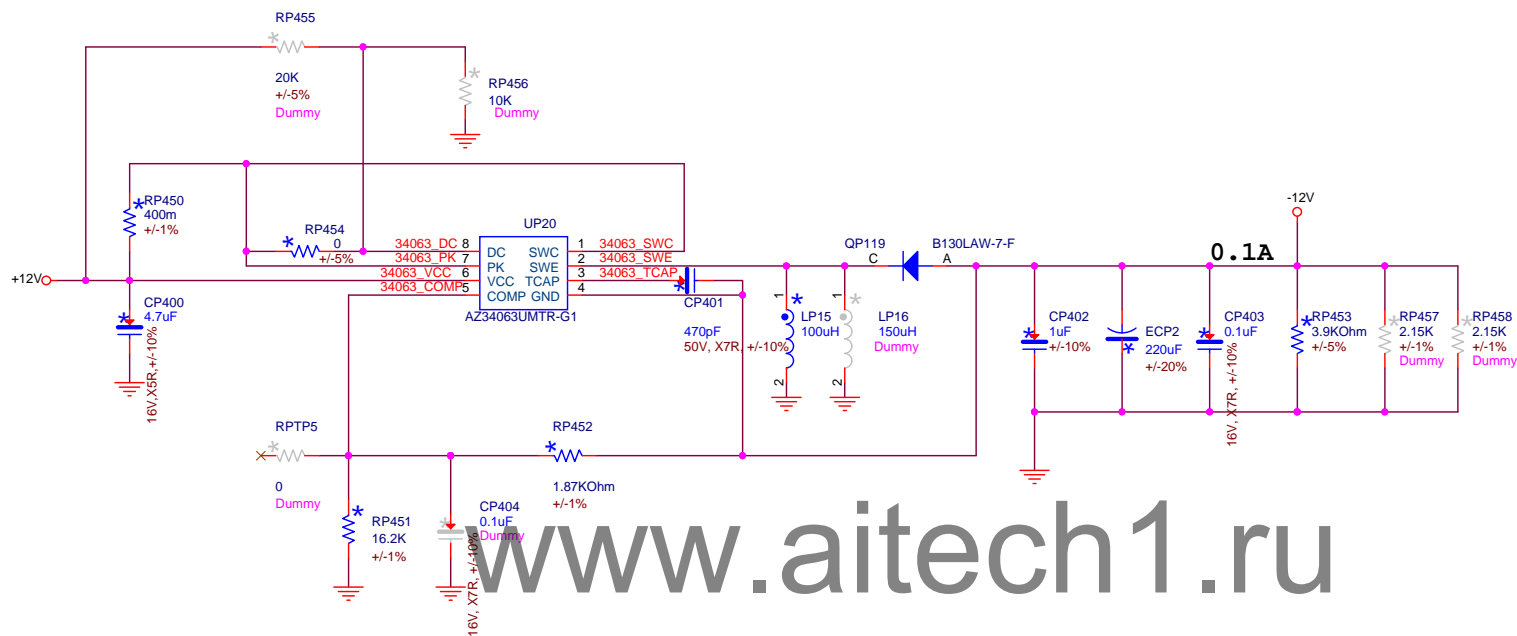
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